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Using Different Versions of ISE

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Document History

1.0	05/05/05	First Written

TABLE OF CONTENTS

For users of FPGA modules there are many example projects provided on the HUNT ENGINEERING CD. These projects are intended to be the starting point when making a new FPGA design with any of the HUNT ENGINEERING FPGA modules. All of the example projects are designed to be used with the standard tool-set provided by Xilinx (there is a separate application note 'Using non ISE development tools' available for users working with development tools such as Leonardo Spectrum or Synplicity).

The standard FPGA design tool from Xilinx is the integrated design environment 'ISE'. Over time Xilinx make improvements to the ISE product and release major version changes. As each new version of design tools is released HUNT ENGINEERING adapt the standard FPGA module examples so they continue to work as expected.

Each time a new version of ISE is released, users may either continue working with their current version of tools, or upgrade to the new version.

Whether continuing with their current version of ISE or upgrading, this document describes what must be done to ensure that the HUNT ENGINEERING FPGA examples continue to work as expected. In addition, this document describes how to make a brand new FPGA project in ISE.

The following three sections describe how to use this document, depending on whether you are upgrading ISE, continuing with your existing version, or making a new project from scratch.

Upgrading to the Latest Version of ISE

The latest version of ISE is version 7.1. The FPGA module examples on the current HUNT ENGINEERING CD are written to use ISE 7.1. For users upgrading to ISE 7.1 this simply means that any of the examples on the *latest* CD can be copied and used without any issue of upgrading the project. In this situation therefore, the remainder of this document does not apply.

However, for users who are upgrading to ISE 7.1, any existing project based around FPGA modules will need to be upgraded.

To upgrade an existing FPGA module project to ISE 7.1 you will need to work through the section 'Upgrading Existing Projects to ISE 7.1'

Continuing to Use a Previous Version of ISE

The latest version of ISE and HUNT ENGINEERING CD examples is version 7.1. If you are continuing to use a version of ISE earlier than ISE 7 and have an existing project then you may continue development without needing to work through the remainder of this document.

If however, you wish to work with any of the new example projects on the current HUNT ENGINEERING CD you will need to work through one of the following sections depending on your current tool version. The section that applies will be one of the following, 'Creating Projects in ISE 4', 'Creating Projects in ISE 5', 'Creating Projects in ISE 6' or 'Creating Projects in ISE 7'.

Creating New Projects

To create a brand new FPGA project in ISE, you will need to work through the appropriate section from either 'Creating Projects in ISE 4', 'Creating Projects in ISE 5', 'Creating Projects in ISE 6' or 'Creating Projects in ISE 7', depending on the version of ISE you are using. You will also need to refer to the 'Making your own FPGA design' section of the User Manual for the FPGA module you are using for module specific information.

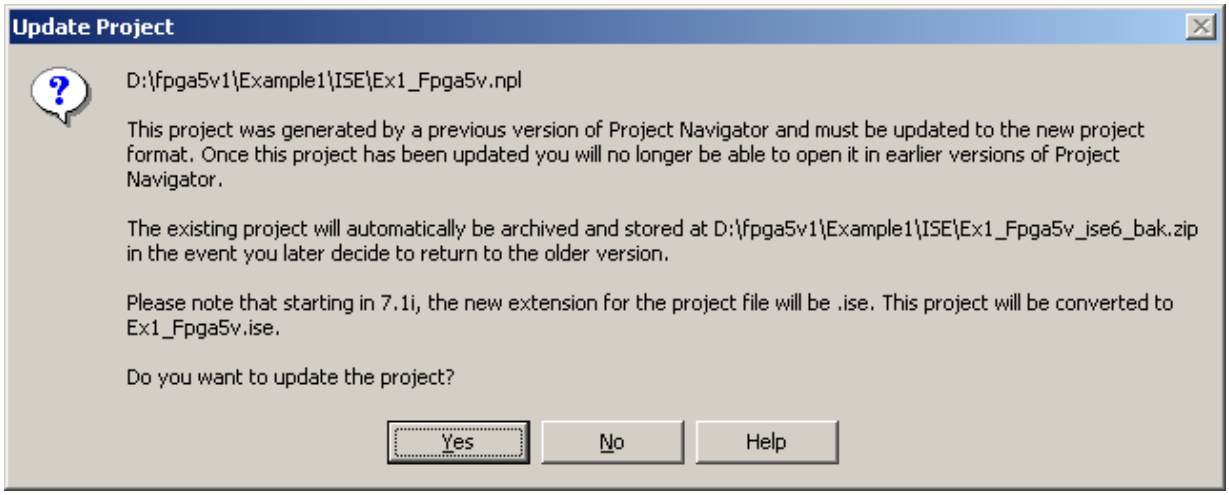
This section describes how to upgrade an existing FPGA module project to work with the latest version of ISE, version 7.1.

The first step in upgrading to ISE 7.1 is to ensure you have installed the latest service pack. In the initial release of ISE 7, the project file import process for converting old projects failed to correctly read the 'Hierarchy Separator' setting in the 'Synthesis Options' of the existing project. This was fixed in Service Pack 1. Please ensure you have completed the installation of the latest service pack before continuing through this section.

The next step in upgrading an existing project is to replace the contents of the 'Common' directory with the latest FPGA support from HUNT ENGINEERING. Using either the latest HUNT ENGINEERING CD or by visiting the User Area of the HUNT ENGINEERING web-site www.hunteng.co.uk download the IP for the version of FPGA module you are using to a directory on your local drive. With this done, replace the contents of the FPGA projects 'Common' directory with the latest 'Common' FPGA IP.

Now you are ready to open the existing project in ISE. Open the ISE 7.1 Project Navigator and click 'File→Open Project…'. Select the project file you wish to open.

You should then see a window similar to that shown below.



This window indicates that the project needs updating. Also note that the project file extension changes from '.npl' to '.ise' with version 7. Click 'Yes' to continue.

You will now be able to continue development on the converted project in ISE 7.1.

For each FPGA module type, each project contained on the CD provides all of the required design elements to ensure correct operation on that chosen module type. These elements include a Hardware Interface Layer that is used to correctly control external devices, user constraints information to control design timing and pin location and example VHDL to provide a structured starting point.

For users of ISE 4 design tools this document must be followed in order to convert the newer project format used on the HUNT ENGINEERING CD to the correct ISE 4 format. This section describes how to build an ISE 4 project from scratch, using the design source provided on the CD. This process is necessary as the standard XILINX tool version has moved on from ISE 4 and XILINX provide no mechanism for converting post ISE 4 projects back to ISE 4.

This document uses Example1 as the starting point for the creation of a new project. It is important to start from one of the standard examples provided on the HUNT ENGINEERING CD as this give the correct starting point for FPGA development with your FPGA module.

Please note: if you are using this section in order to create a brand new project with functionality that does not match any of the standard CD examples, then you must still start from Example1. Once you have created a correct project based around Example1 you may then insert your own unique code into the User-Ap entity, removing all unwanted logic. When doing this, you will need to refer to the relevant information in the ‘Making your own FPGA design’ section of your FPGA User Manual.

Converting Example1 for your Module Type

The HUNT ENGINEERING CD provides support for many different FPGA module types. For each module there is always a standard Example1 project provided on the CD. This example is the 'Getting Started' example for each module type and should always be used as the first step in FPGA development.

This section describes how to convert Example1 for the HERON-FPGA5 as an example of the conversion process. Although the design source varies for each module type, the principles shown here are the same regardless of type.

Step 1: Copying Example1 from the HUNT ENGINEERING CD

The first step in the conversion process is to copy Example1 onto your local hard drive. Make a directory on your local drive in which to store Example1.

On the HUNT ENGINEERING CD, all FPGA examples are provided below the 'fpga' directory. The 'fpga' directory is divided into sub-directories that reflect the name of the module type. In this document, Example1 for the HERON-FPGA5 is to be converted, so the directory 'fpga/fpga5v1/' will contain the appropriate project information. Identify the appropriate CD directory according to your module type.

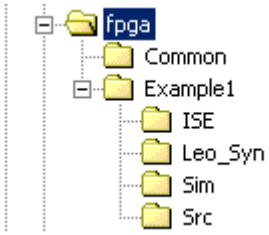
With the correct CD directory located you will need to copy Example 1 to your local drive. This can be done in one of two ways. The first method is to copy the Example 1 project by hand for the module type you are using. The second method is to unzip the ZIP file for that module type onto your hard drive.

When using the first approach you will need to copy the 'Common' directory and 'Example1' directory from the CD to a chosen directory on your local drive. The 'Example1' directory contains all design source that forms Example1 and the 'Common' directory provides design source common to all designs made for that module.

Please note, when copying files from your CD by hand you may need to edit the file attributes after copying. This is because on some operating systems Read-Only files on the CD will become Read-Only files on your local drive. All files in the 'Example1' directory should be set to Read-Write while all files in the 'Common' directory must remain Read-Only.

When using the second approach you will be unzipping all examples for that module, including Example1. When unzipping all project examples, the read-write attributes will automatically be set correctly.

The picture below shows a new directory on the local drive named 'fpga'. In the 'fpga' directory are the copied 'Common' and 'Example1' directories.



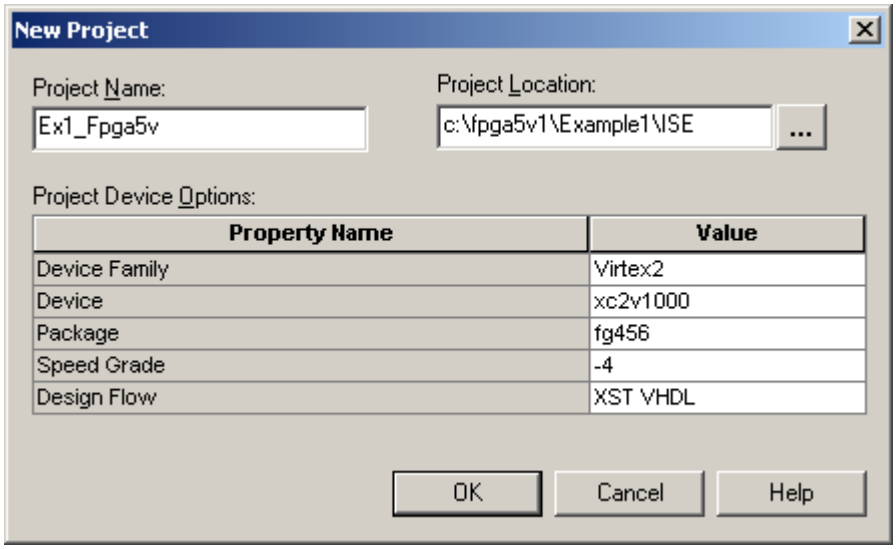
Step 2: Creating a New Project File

With the Example1 example directory and Common directory copied onto your Local Drive you can now begin building an ISE 4 project.

Open the ISE 4 Project Navigator if it is not already open. Please note, in the remainder of this section an example conversion is shown for Example 1 for the HERON-FPGA5 where this conversion is performed in ISE 4.1. If you are using a different ISE 4 version then although the windows shown may not perfectly match, the conversion process is still the same.

Next, delete the project file for the Example1 project in the new directory you have created on your local drive. The project file will be located in the 'ISE' sub-directory of the 'Example1' directory and will have the extension '.ise'. This existing project file must be removed as it will not be useable in ISE 4 and must be replaced with an appropriately constructed project file.

With the existing file deleted, select the menu item 'File→New Project…' to begin creating a new project. The following window should be displayed.



Enter the correct project name in the 'Project Name' field. For Example1 this should be set to be the same project name as the Example1 project file on the HUNT ENGINEERING CD (minus the .ise extension).

Next, enter the correct location into the 'Project Location' field. This field should match the location of the 'Example1/ISE' directory you have made on your local drive.

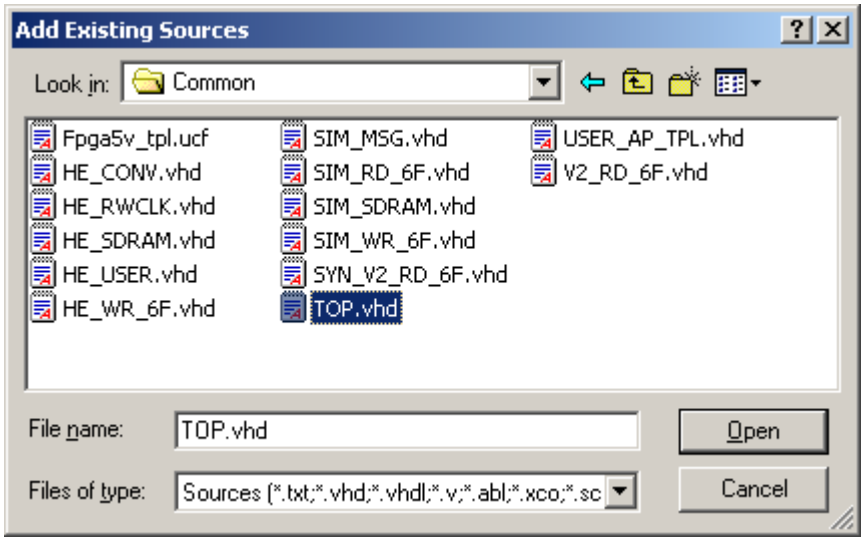
Then set the Project Device Options to correctly reflect the appropriate device information according to the module type you are using. If you are unsure of the correct information refer to the User Manual for that module type. Ensure that the Design Flow is 'XST VHDL'.

When you have correctly defined all fields click 'OK'.

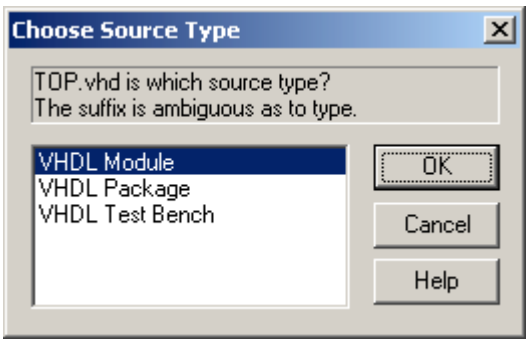
Step 3: Adding VHDL Source to the New Project

The next step is to add design source, starting with the top level of the hierarchy. For all FPGA module projects the top level of the design is always contained in the file 'top.vhd'. 'top.vhd' is always provided as part of the 'Common' directory for each module type.

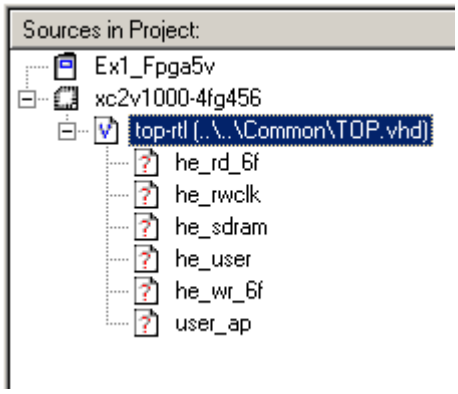
Select the menu item 'Project→Add Source…'. The following window will be displayed where you will need to navigate to the 'Common' directory that was created on your local drive. Select the file 'top.vhd' and click 'Open'.



The following window will then appear. Select 'VHDL Module' and click OK to add 'top.vhd' to the project.



With this done, the Module View window will now look similar to the picture below, depending on the particular source files that are required by the module type you are using:



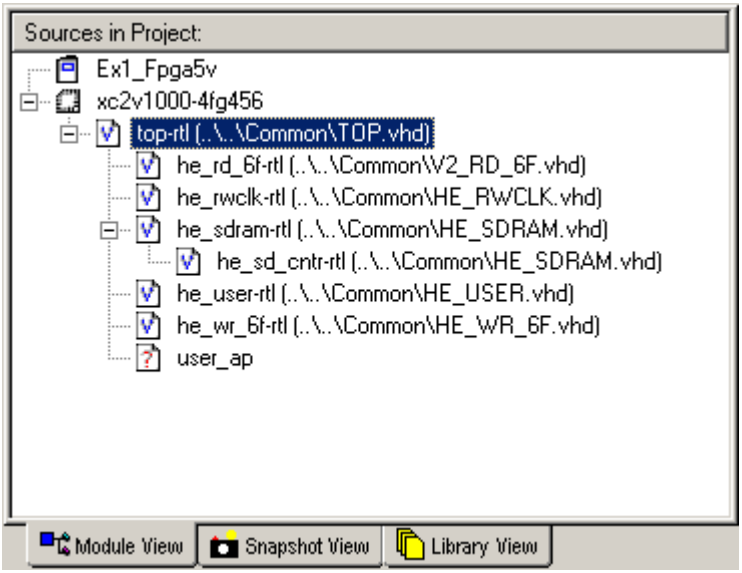
In the case of the FPGA5v1 example conversion, after adding 'top.vhd' we can now see 6 more design entities are needed. One of these entities is the User-Application level of the design which contains the VHDL that makes this example the getting started example, Example1. The other entities shown are part of the Hardware Interface Layer and are found in the 'Common' directory.

First add the appropriate files from the 'Common' directory in order to replace the red question mark icons with correct entities. To do this, you will again need to use the 'Add Source…' menu item. Navigate to the 'Common' directory and select the files that have names that match the entities in the Module View of your new project.

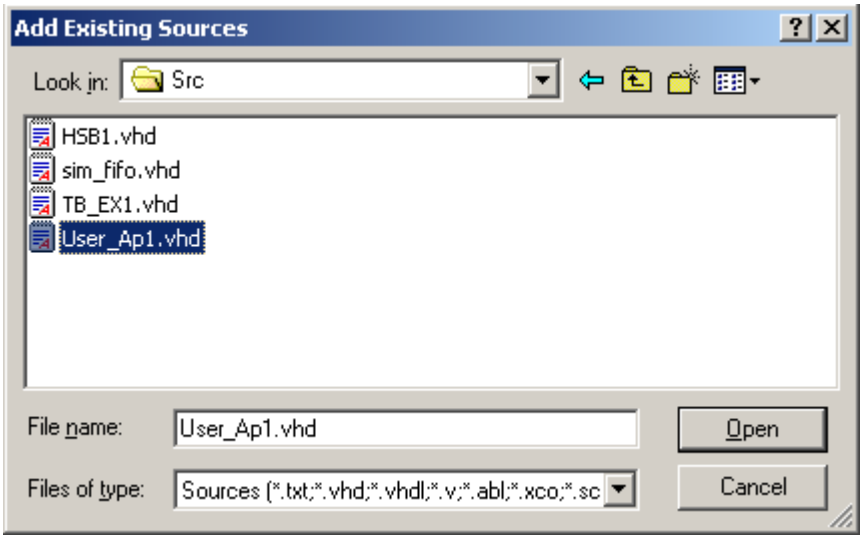
Please note: the HE_RD_6F entity is provided in the 'Common' directory in the source file 'V2_RD_6F'.

When adding each file, the correct Source Type will be 'VHDL Module' as was selected when adding 'top.vhd'.

When you have added all required Hardware Interface Layer components the Module View should look similar to the picture below for the FPGA5v1 conversion:



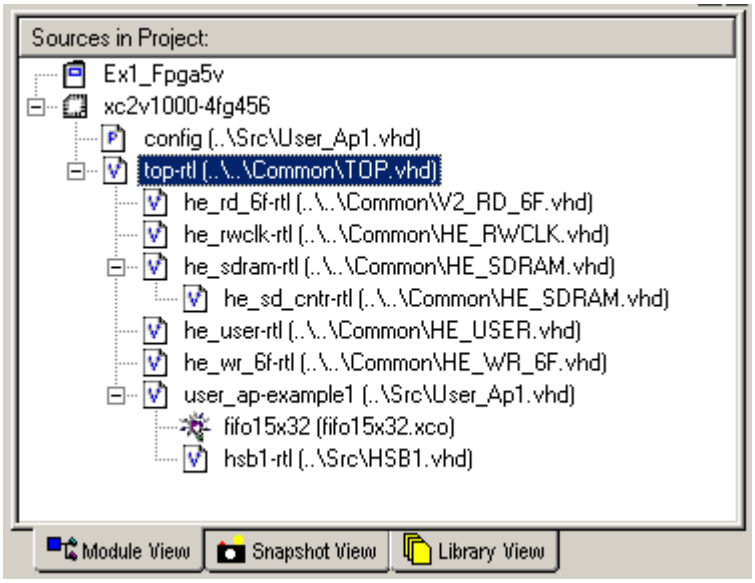
Next you will need to navigate to the ‘Src’ directory of Example1 and add the User_Ap file to the project:



After the ‘user_ap’ entity has been added to the project you will see which other source files are required below this entity. Add the appropriate source files from the ‘Src’ directory.

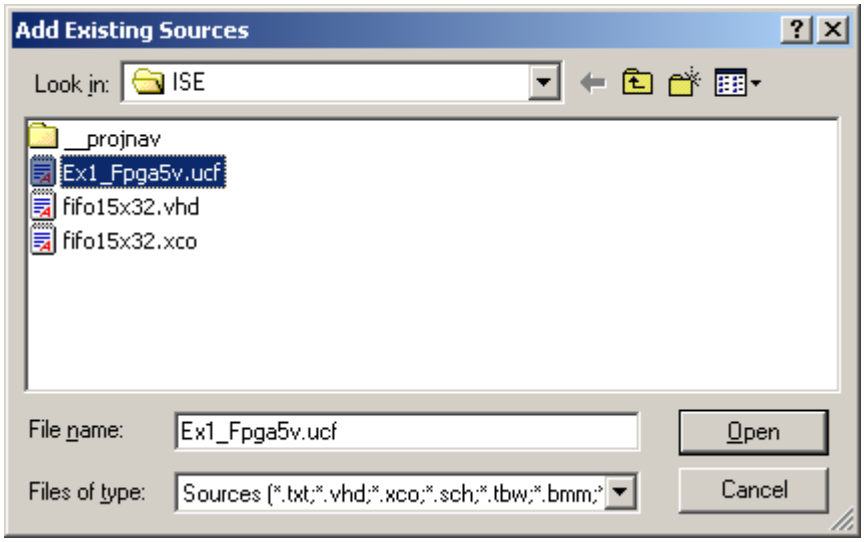
After you have added all of required VHDL source files from the ‘Src’ directory there may still be red question marks against entities in the hierarchy. These entities will correspond to Core Gen components that are placed in the Example1 ‘ISE’ directory. In the case of Example1 there is one Core Gen component called ‘fifo15x32’ that must be added to the project from the ‘ISE’ directory.

With all relevant VHDL source added to the project the Module View should look similar to the picture shown below for the FPGA5v1 conversion:

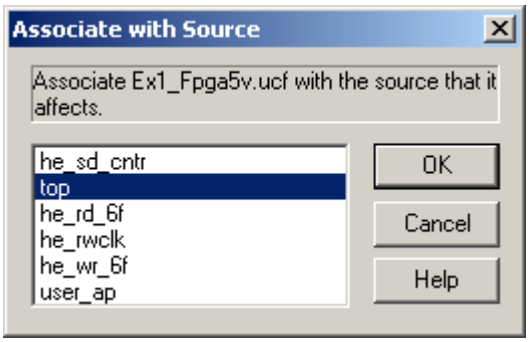


Step 4: Adding User Constraints

The next step is to add user design constraints to the project. Using 'Project→Add Source…' add the user constraints file contained in the 'ISE' directory of the project.

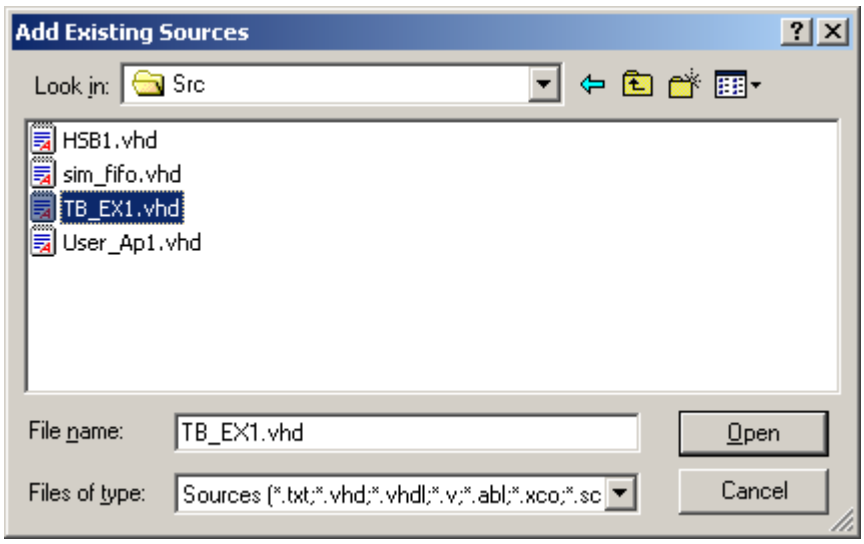


Select the UCF file and click 'Open'. The following window will appear to allow you to specify the design file to which the user constraints should be associated. Highlight 'top' and click 'OK'.

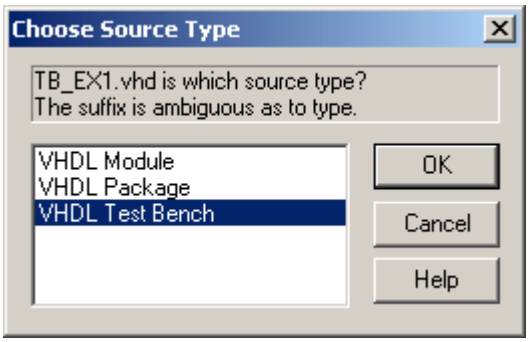


Step 5: Adding a Simulation Test-Bench

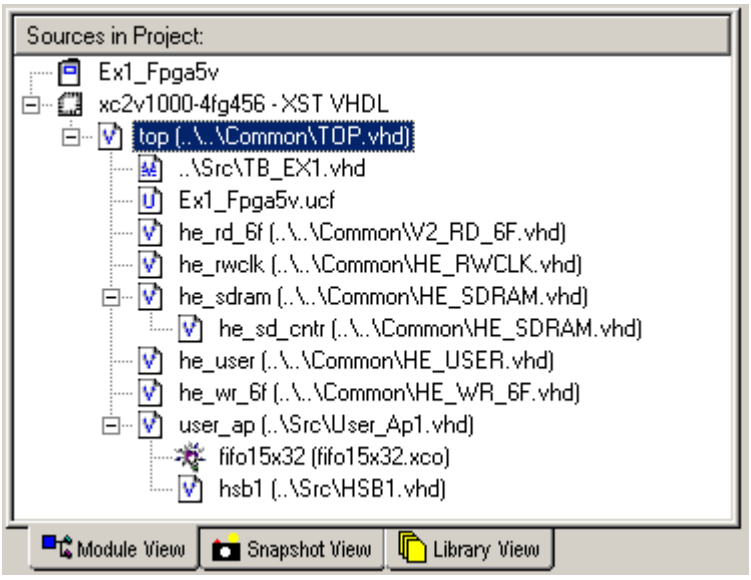
Typically, a project will also include a test-bench for simulation. For Example1 there is a test-bench provided in the 'Src' directory of the project. This file must also be added to the project using 'Project→Add Source…'. Navigate to the 'Src' directory, highlight the file that beings 'TB_' and click 'Open'.



The following window will appear where you need to specify the source type. Select 'VHDL Test Bench' and click 'OK'.



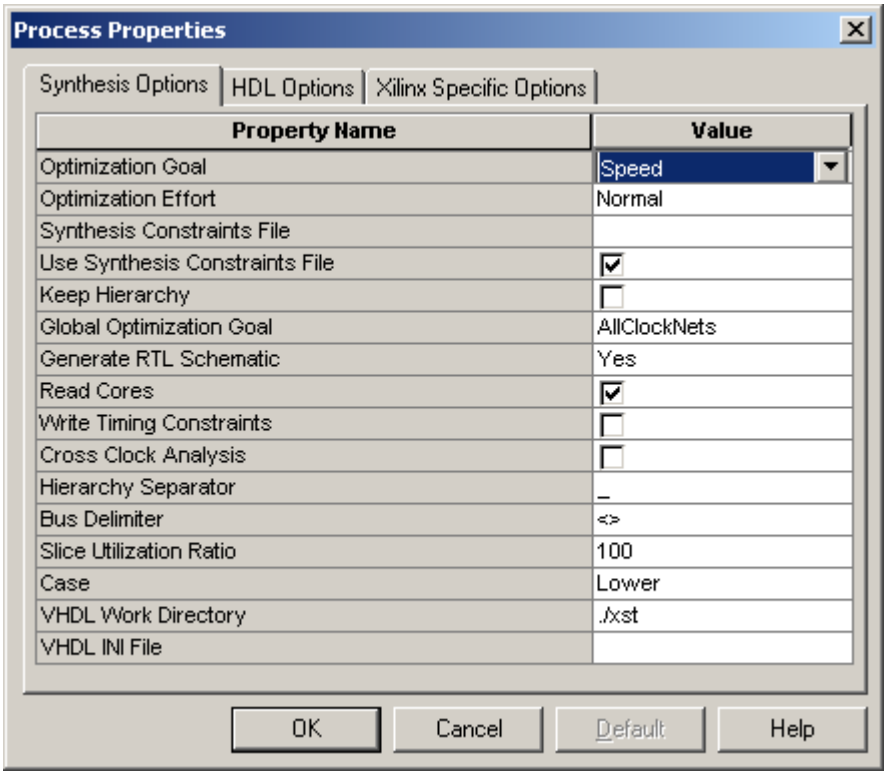
At this point the Module View should look similar to the picture shown below for the FPGA5v1 conversion process.



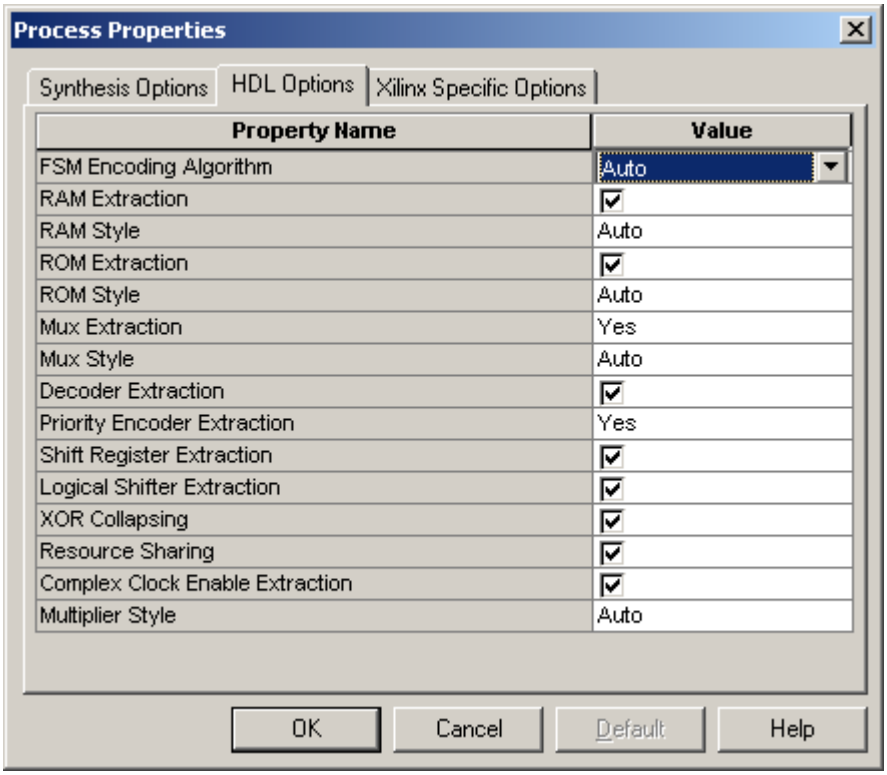
Step 6: Setting Project Build Options

The last step in creating a new project is to apply the necessary project settings that will allow the design to be built correctly.

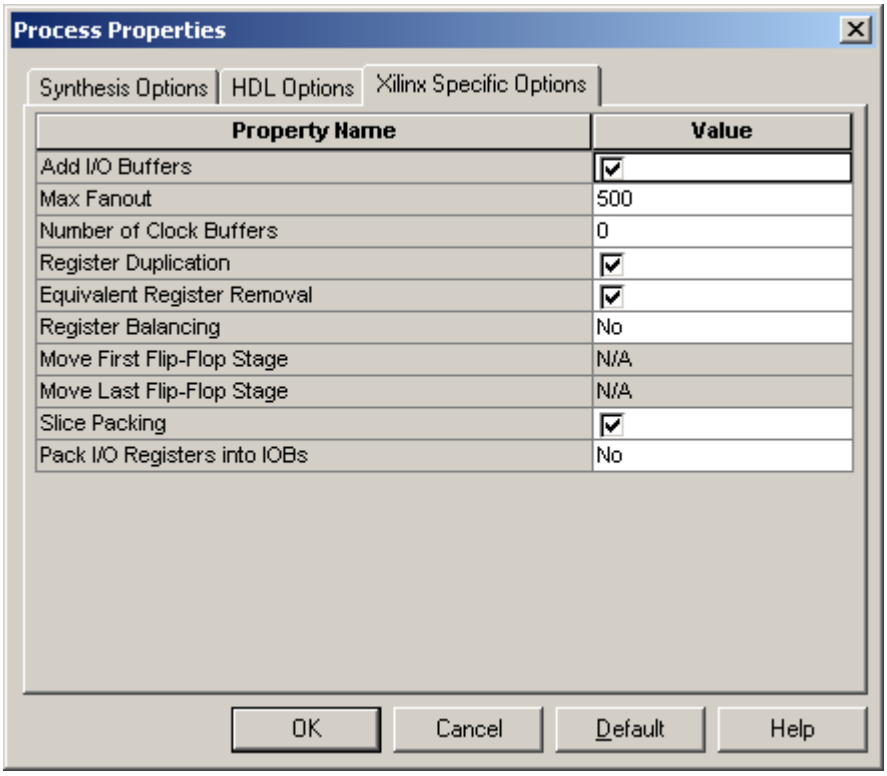
Ensure the file 'top.vhd' is highlighted in the Module View, and then right click on 'Synthesize' in the Process View. Select 'Properties…' to open the following window. With the 'Synthesis Options' tab at the front, check that the settings match those shown below.



Next bring the ‘HDL Options’ tab to the front and check that the settings match those in the picture below.

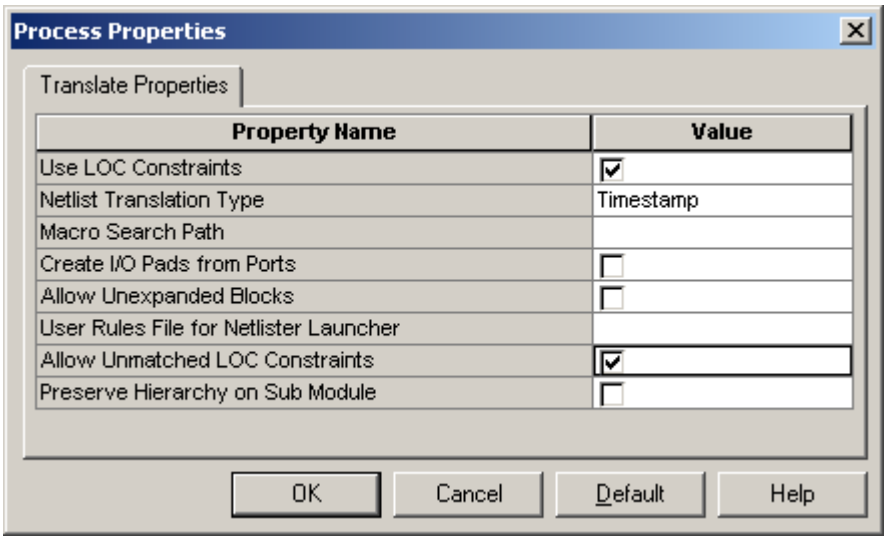


Next bring the ‘Xilinx Specific Options’ tab to the front. Change the ‘Number of Clock Buffers’ item to ‘0’, and set the ‘Pack I/O Registers into IOBs’ item to ‘No’. With this done, check that the settings match those in the picture below.

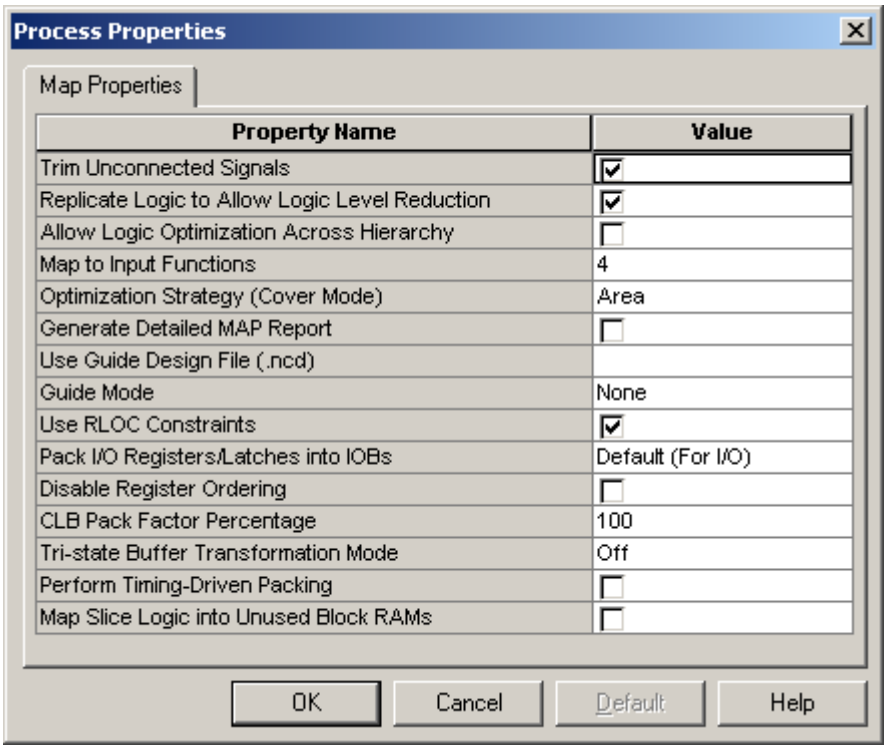


Click on the ‘OK’ button at the bottom of the window to apply the new settings.

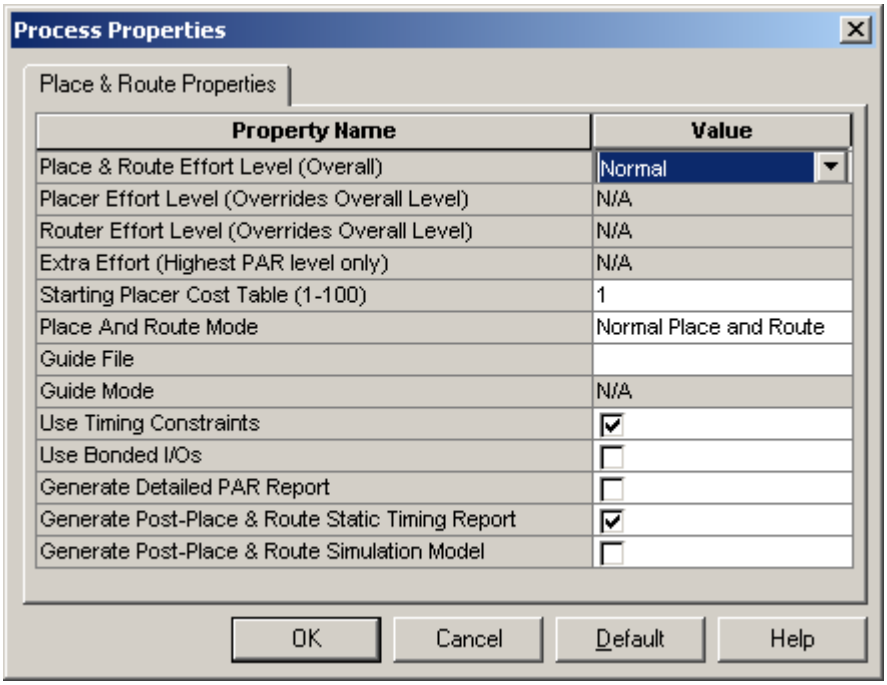
Next the Translate Properties must be checked. With the file ‘top.vhd’ still highlighted in the Module View right click on ‘Translate’ in the Process View. Select ‘Properties…’ to open the following window. Tick the item ‘Allow Unmatched LOC Constraints’, check all other settings match, and click ‘OK’.



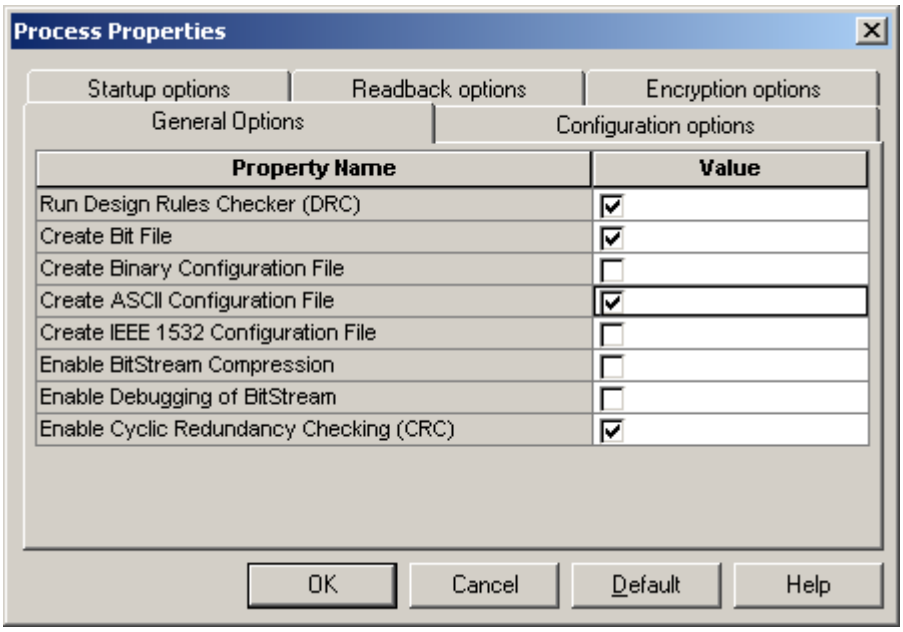
Next open the Process Properties window for the Map process. Check that the settings match those in the picture below.



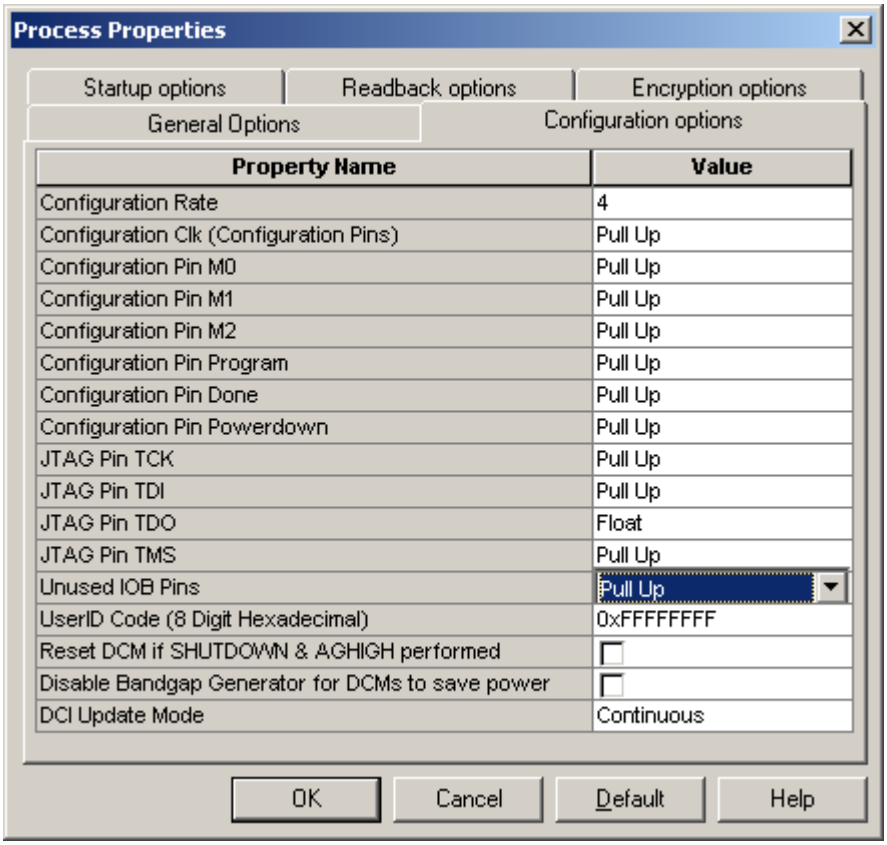
Next check the Place and Route process properties. For Example1 the 'Place & Route Effort Level (Overall)' typically needs to be set to 'Normal'. Make this change and check all other settings match the picture below and click 'OK'.



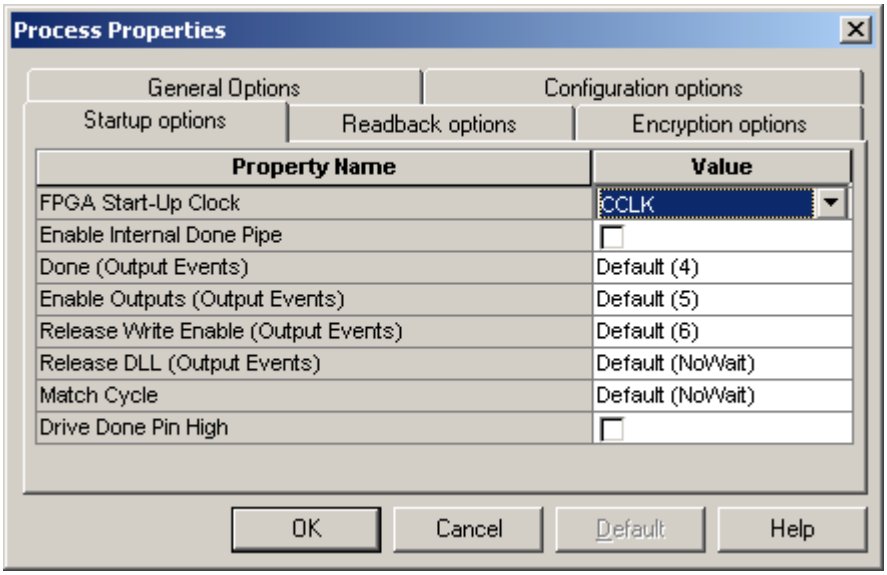
Next check the 'Generate Programming File' properties. With the 'General Options' tab at the front, tick the 'Create ASCII Configuration File' and then check that all other settings match for this tab.



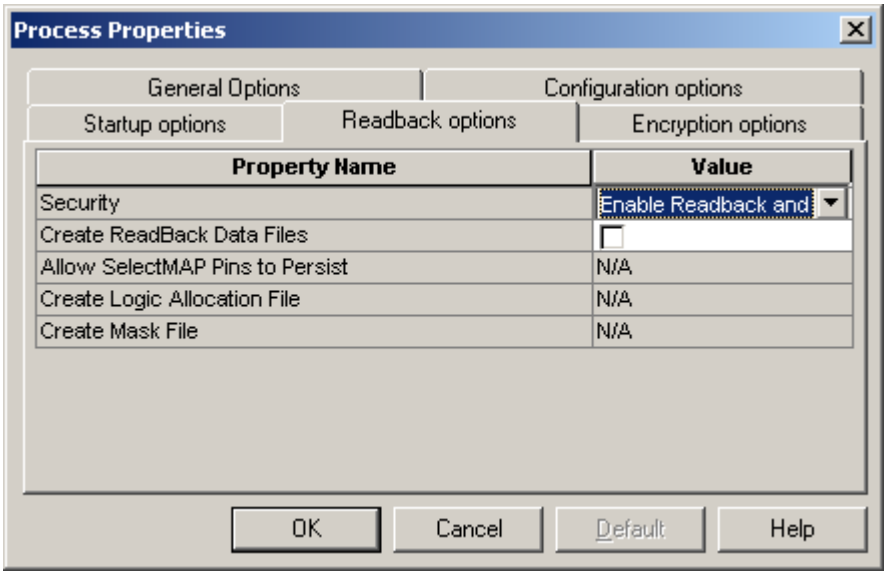
Bring the Configuration Options to the front. Select ‘Pull Up’ for the ‘Unused IOB Pins’ item. With this done check the settings match those shown in the picture below.



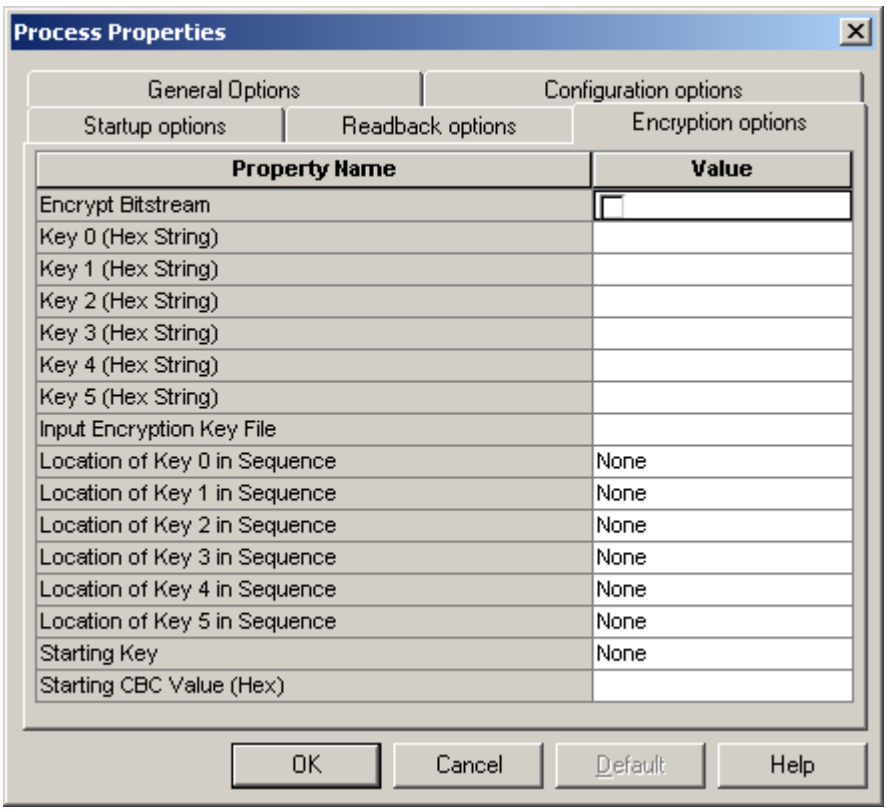
Next check the settings for the ‘Startup Options’ tab against those shown in the picture below.



Next check the ‘Readback Options’ against the picture below.



Finally check the ‘Encryption Options’ tab against the picture shown below.



When all tabs have been checked, click ‘OK’ to enter the new settings.

Step 7: Building the Project

At this point the project is ready to be built. All of the required design files have been added to the project and the project build settings have been checked. Example1 should now build as far as bitstream generation without error.

Although each example project supplied on the HUNT ENGINEERING CD will differ from Example1, the process to create a new project for ISE 4 is the same. The routine described in this section can therefore be repeated for each of the standard examples provided on the CD.

For each FPGA module type, each project contained on the CD provides all of the required design elements to ensure correct operation on that chosen module type. These elements include a Hardware Interface Layer that is used to correctly control external devices, user constraints information to control design timing and pin location and example VHDL to provide a structured starting point.

For users of ISE 5 design tools this document must be followed in order to convert the newer project format used on the HUNT ENGINEERING CD to the correct ISE 5 format. This section describes how to build an ISE 5 project from scratch, using the design source provided on the CD. This process is necessary as the standard XILINX tool version has moved on from ISE 5 and XILINX provide no mechanism for converting post ISE 5 projects back to ISE 5.

This document uses Example1 as the starting point for the creation of a new project. It is important to start from one of the standard examples provided on the HUNT ENGINEERING CD as this give the correct starting point for FPGA development with your FPGA module.

Please note: if you are using this section in order to create a brand new project with functionality that does not match any of the standard CD examples, then you must still start from Example1. Once you have created a correct project based around Example1 you may then insert your own unique code into the User-Ap entity, removing all unwanted logic. When doing this, you will need to refer to the relevant information in the ‘Making your own FPGA design’ section of your FPGA User Manual.

Converting Example1 for your Module Type

The HUNT ENGINEERING CD provides support for many different FPGA module types. For each module there is always a standard Example1 project provided on the CD. This example is the 'Getting Started' example for each module type and should always be used as the first step in FPGA development.

This section describes how to convert Example1 for the HERON-FPGA5 as an example of the conversion process. Although the design source varies for each module type, the principles shown here are the same regardless of type.

Step 1: Copying Example1 from the HUNT ENGINEERING CD

The first step in the conversion process is to copy Example1 onto your local hard drive. Make a directory on your local drive in which to store Example1.

On the HUNT ENGINEERING CD, all FPGA examples are provided below the 'fpga' directory. The 'fpga' directory is divided into sub-directories that reflect the name of the module type. In this document, Example1 for the HERON-FPGA5 is to be converted, so the directory 'fpga/fpga5v1/' will contain the appropriate project information. Identify the appropriate CD directory according to your module type.

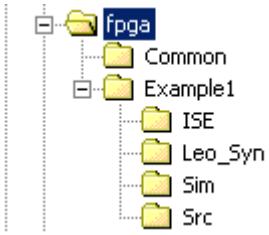
With the correct CD directory located you will need to copy Example 1 to your local drive. This can be done in one of two ways. The first method is to copy the Example 1 project by hand for the module type you are using. The second method is to unzip the ZIP file for that module type onto your hard drive.

When using the first approach you will need to copy the 'Common' directory and 'Example1' directory from the CD to a chosen directory on your local drive. The 'Example1' directory contains all design source that forms Example1 and the 'Common' directory provides design source common to all designs made for that module.

Please note, when copying files from your CD by hand you may need to edit the file attributes after copying. This is because on some operating systems Read-Only files on the CD will become Read-Only files on your local drive. All files in the 'Example1' directory should be set to Read-Write while all files in the 'Common' directory must remain Read-Only.

When using the second approach you will be unzipping all examples for that module, including Example1. When unzipping all project examples, the read-write attributes will automatically be set correctly.

The picture below shows a new directory on the local drive named 'fpga'. In the 'fpga' directory are the copied 'Common' and 'Example1' directories.



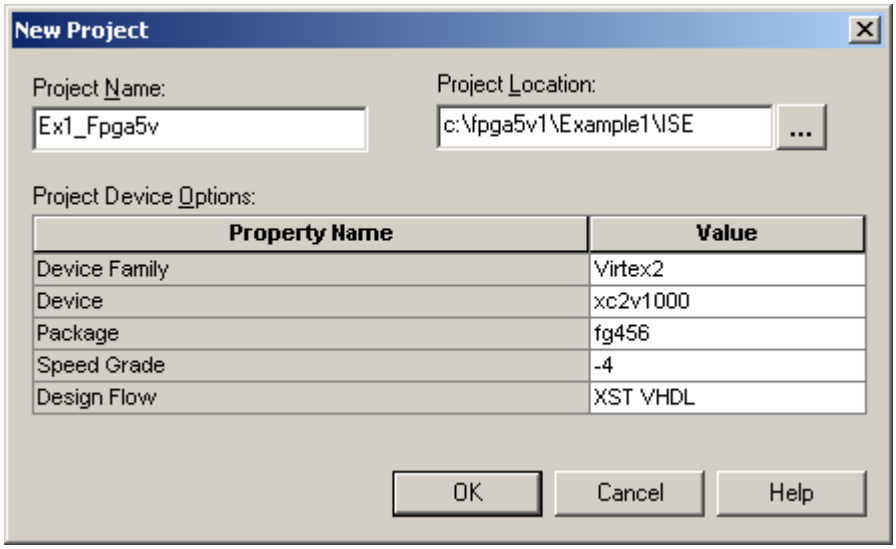
Step 2: Creating a New Project File

With the Example1 example directory and Common directory copied onto your Local Drive you can now begin building an ISE 5 project.

Open the ISE 5 Project Navigator if it is not already open. Please note, in the remainder of this section an example conversion is shown for Example 1 for the HERON-FPGA5 where this conversion is performed in ISE 5.2. If you are using a different ISE 5 version then although the windows shown may not perfectly match, the conversion process is still the same.

Next, delete the project file for the Example1 project in the new directory you have created on your local drive. The project file will be located in the 'ISE' sub-directory of the 'Example1' directory and will have the extension '.ise'. This existing project file must be removed as it will not be useable in ISE 5 and must be replaced with an appropriately constructed project file.

With the existing file deleted, select the menu item 'File→New Project…' to begin creating a new project. The following window should be displayed.



Enter the correct project name in the 'Project Name' field. For Example1 this should be set to be the same project name as the Example1 project file on the HUNT ENGINEERING CD (minus the .ise extension).

Next, enter the correct location into the 'Project Location' field. This field should match the location of the 'Example1/ISE' directory you have made on your local drive.

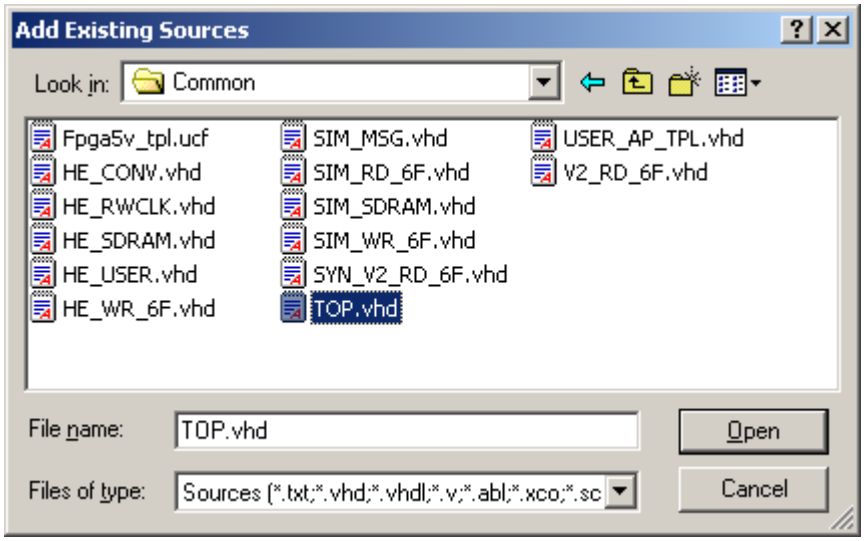
Then set the Project Device Options to correctly reflect the appropriate device information according to the module type you are using. If you are unsure of the correct information refer to the User Manual for that module type. Ensure that the Design Flow is 'XST VHDL'.

When you have correctly defined all fields click 'OK'.

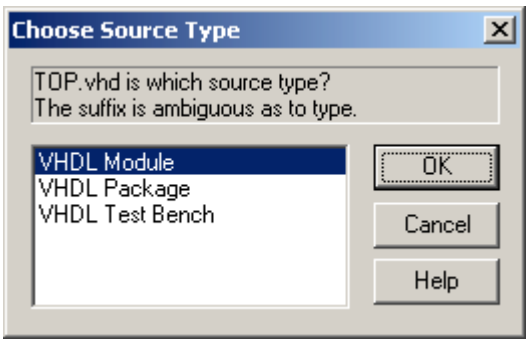
Step 3: Adding VHDL Source to the New Project

The next step is to add design source, starting with the top level of the hierarchy. For all FPGA module projects the top level of the design is always contained in the file 'top.vhd'. 'top.vhd' is always provided as part of the 'Common' directory for each module type.

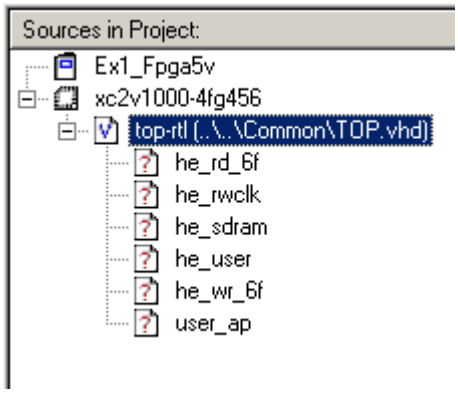
Select the menu item 'Project→Add Source…'. The following window will be displayed where you will need to navigate to the 'Common' directory that was created on your local drive. Select the file 'top.vhd' and click 'Open'.



The following window will then appear. Select 'VHDL Module' and click OK to add 'top.vhd' to the project.



With this done, the Module View window will now look similar to the picture below, depending on the particular source files that are required by the module type you are using:



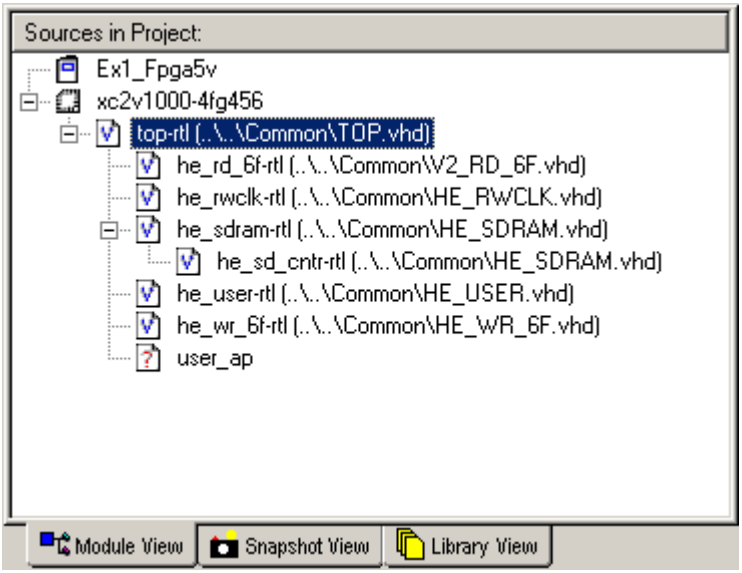
In the case of the FPGA5v1 example conversion, after adding 'top.vhd' we can now see 6 more design entities are needed. One of these entities is the User-Application level of the design which contains the VHDL that makes this example the getting started example, Example1. The other entities shown are part of the Hardware Interface Layer and are found in the 'Common' directory.

First add the appropriate files from the 'Common' directory in order to replace the red question mark icons with correct entities. To do this, you will again need to use the 'Add Source…' menu item. Navigate to the 'Common' directory and select the files that have names that match the entities in the Module View of your new project.

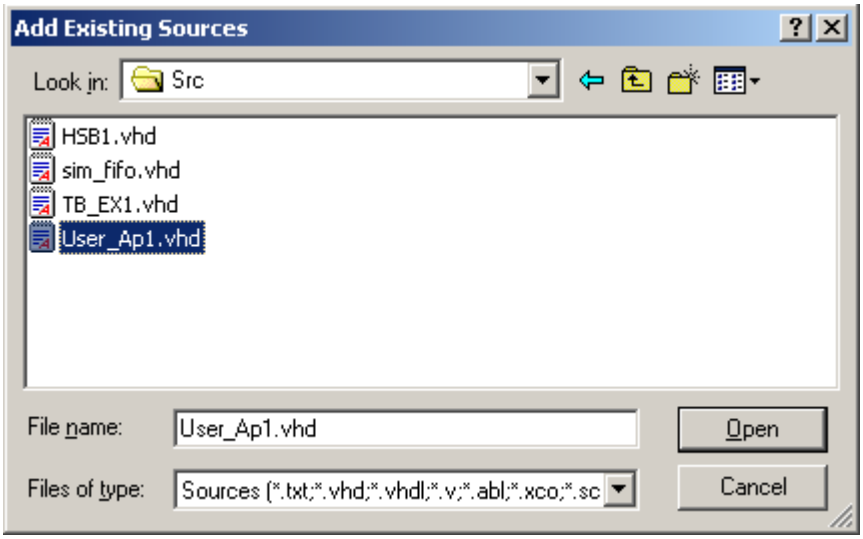
Please note: the HE_RD_6F entity is provided in the 'Common' directory in the source file 'V2_RD_6F'.

When adding each file, the correct Source Type will be 'VHDL Module' as was selected when adding 'top.vhd'.

When you have added all required Hardware Interface Layer components the Module View should look similar to the picture below for the FPGA5v1 conversion:



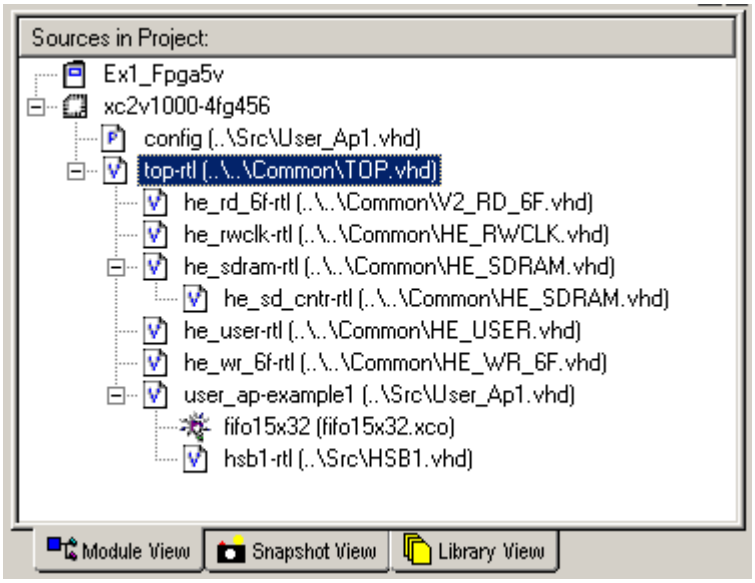
Next you will need to navigate to the ‘Src’ directory of Example1 and add the User_Ap file to the project:



After the ‘user_ap’ entity has been added to the project you will see which other source files are required below this entity. Add the appropriate source files from the ‘Src’ directory.

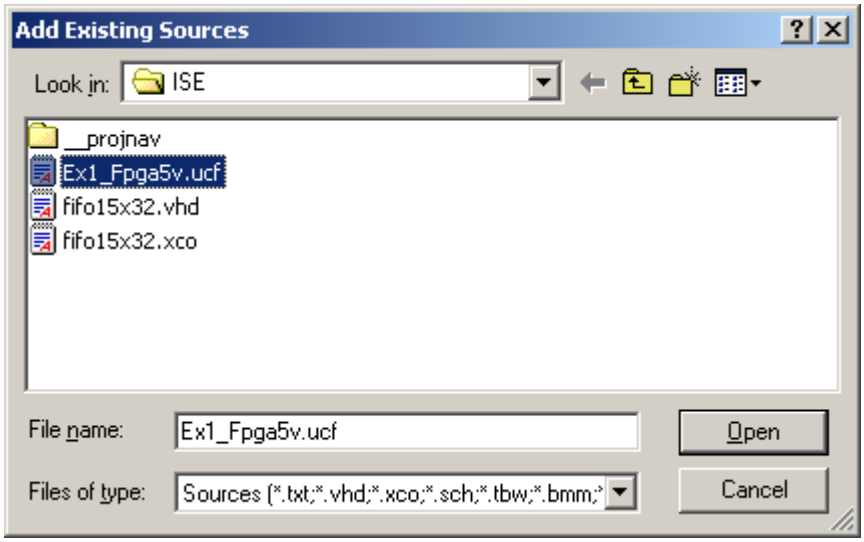
After you have added all of required VHDL source files from the ‘Src’ directory there may still be red question marks against entities in the hierarchy. These entities will correspond to Core Gen components that are placed in the Example1 ‘ISE’ directory. In the case of Example1 there is one Core Gen component called ‘fifo15x32’ that must be added to the project from the ‘ISE’ directory.

With all relevant VHDL source added to the project the Module View should look similar to the picture shown below for the FPGA5v1 conversion:

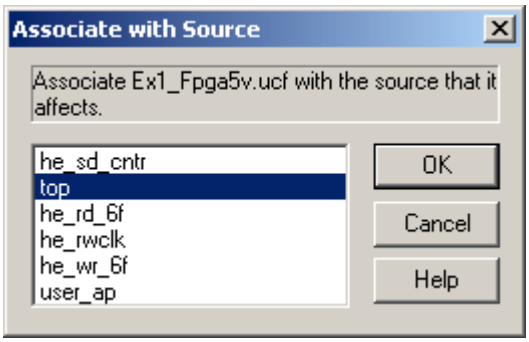


Step 4: Adding User Constraints

The next step is to add user design constraints to the project. Using 'Project→Add Source…' add the user constraints file contained in the 'ISE' directory of the project.

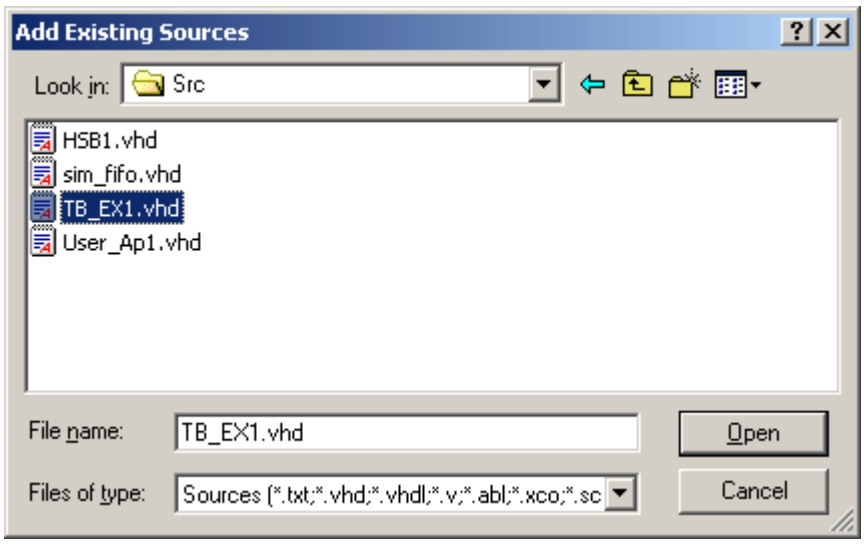


Select the UCF file and click 'Open'. The following window will appear to allow you to specify the design file to which the user constraints should be associated. Highlight 'top' and click 'OK'.

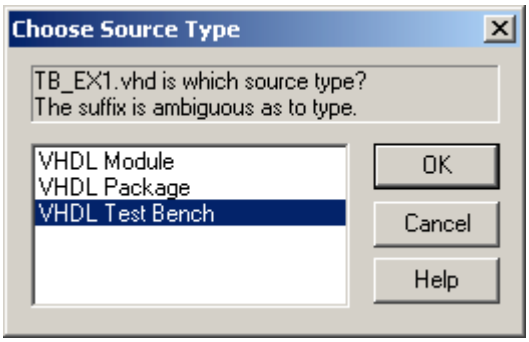


Step 5: Adding a Simulation Test-Bench

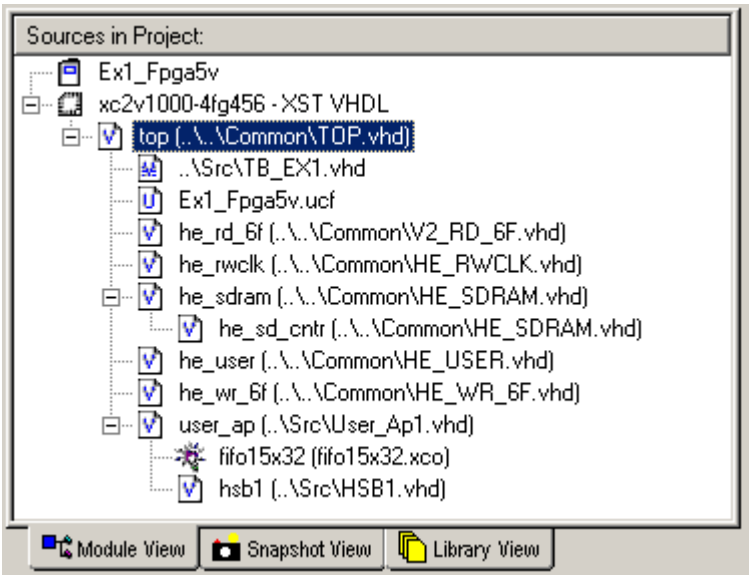
Typically, a project will also include a test-bench for simulation. For Example1 there is a test-bench provided in the 'Src' directory of the project. This file must also be added to the project using 'Project→Add Source…'. Navigate to the 'Src' directory, highlight the file that beings 'TB_' and click 'Open'.



The following window will appear where you need to specify the source type. Select 'VHDL Test Bench' and click 'OK'.



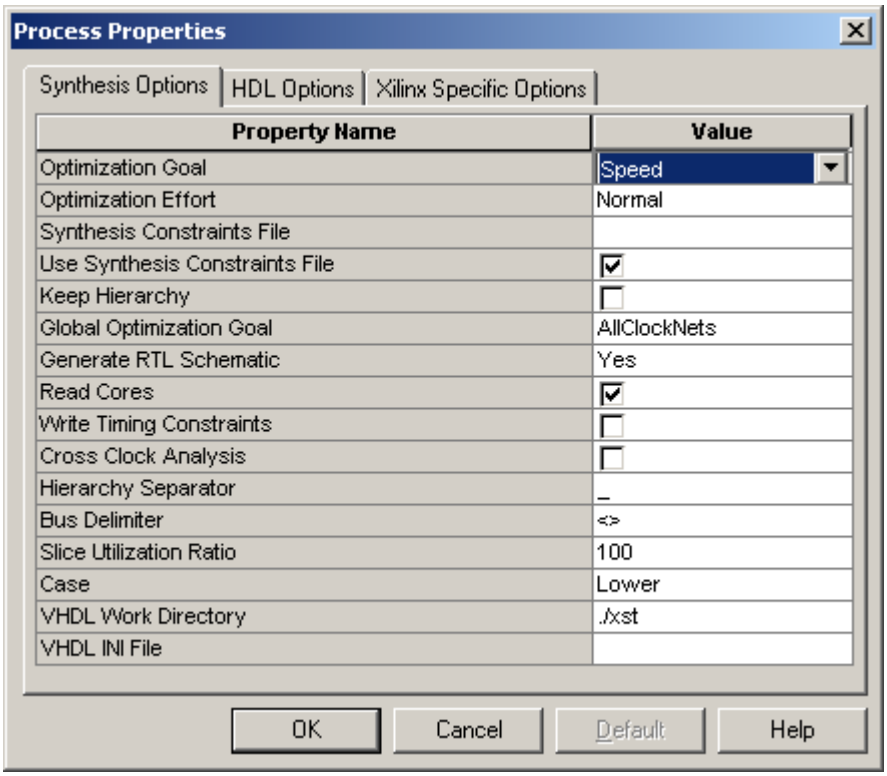
At this point the Module View should look similar to the picture shown below for the FPGA5v1 conversion process.



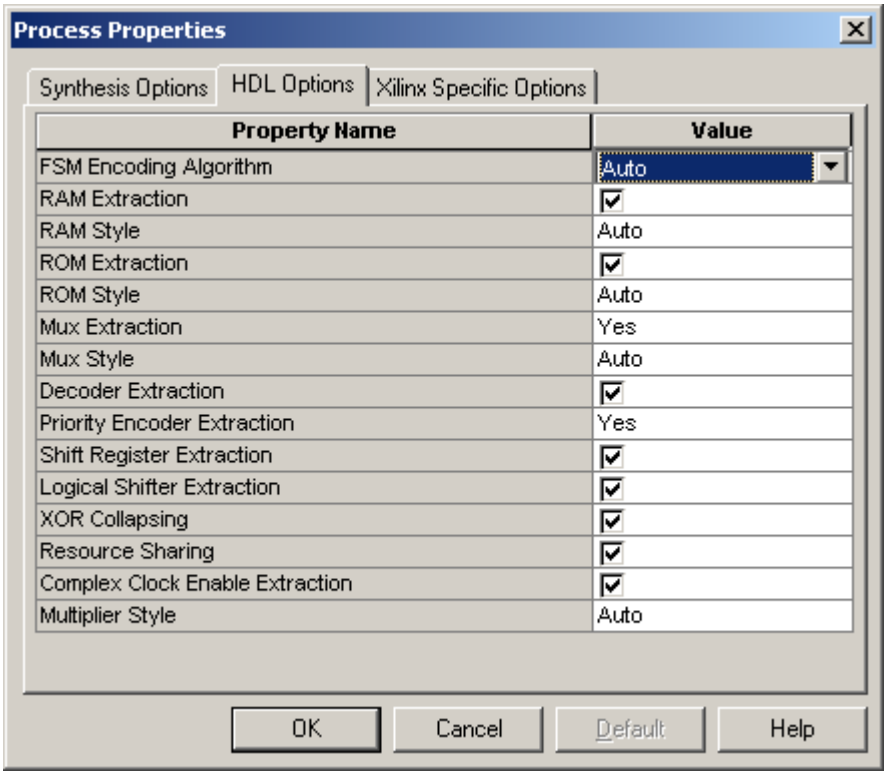
Step 6: Setting Project Build Options

The last step in creating a new project is to apply the necessary project settings that will allow the design to be built correctly.

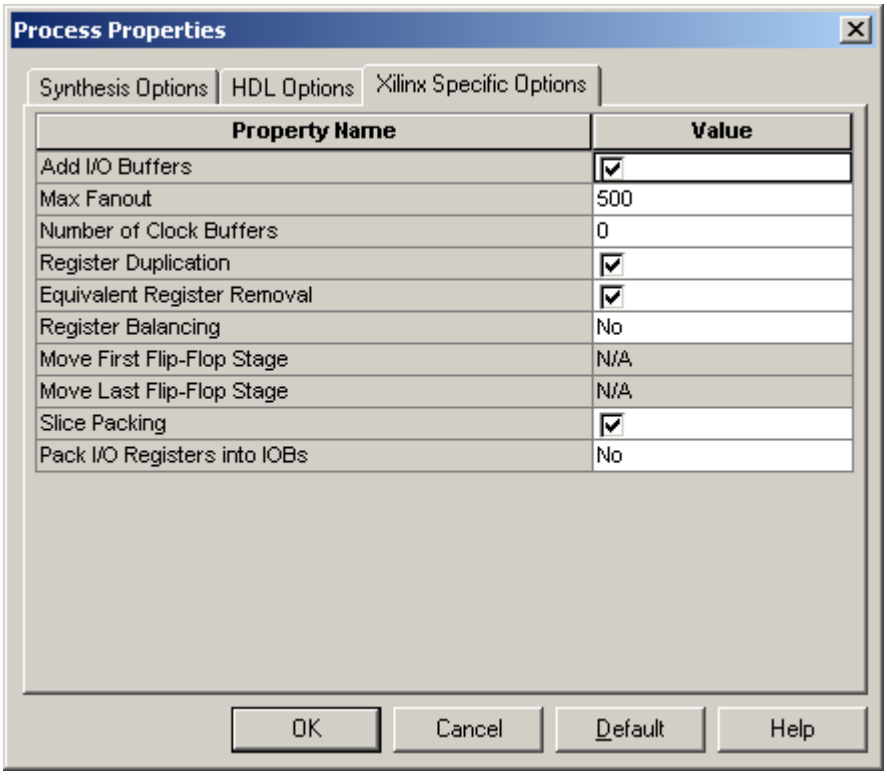
Ensure the file 'top.vhd' is highlighted in the Module View, and then right click on 'Synthesize' in the Process View. Select 'Properties…' to open the following window. With the 'Synthesis Options' tab at the front, check that the settings match those shown below.



Next bring the ‘HDL Options’ tab to the front and check that the settings match those in the picture below.

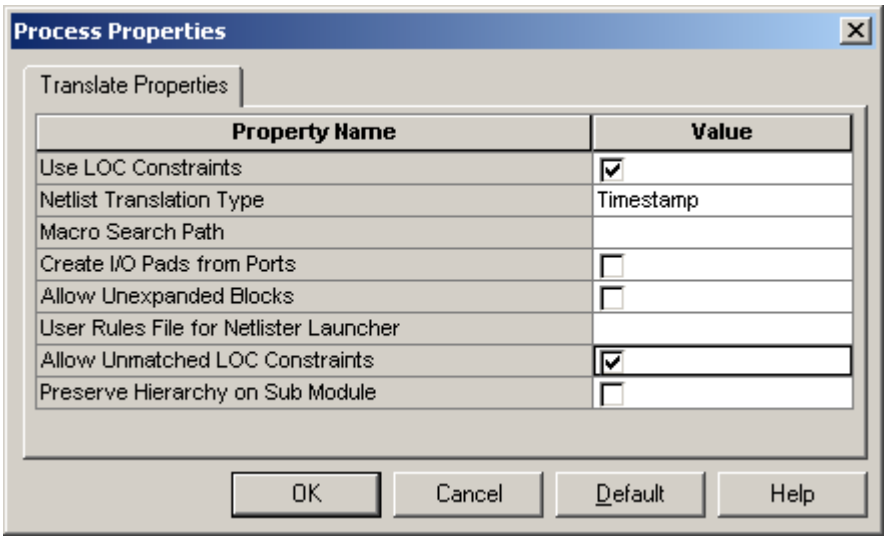


Next bring the ‘Xilinx Specific Options’ tab to the front. Change the ‘Number of Clock Buffers’ item to ‘0’, and set the ‘Pack I/O Registers into IOBs’ item to ‘No’. With this done, check that the settings match those in the picture below.

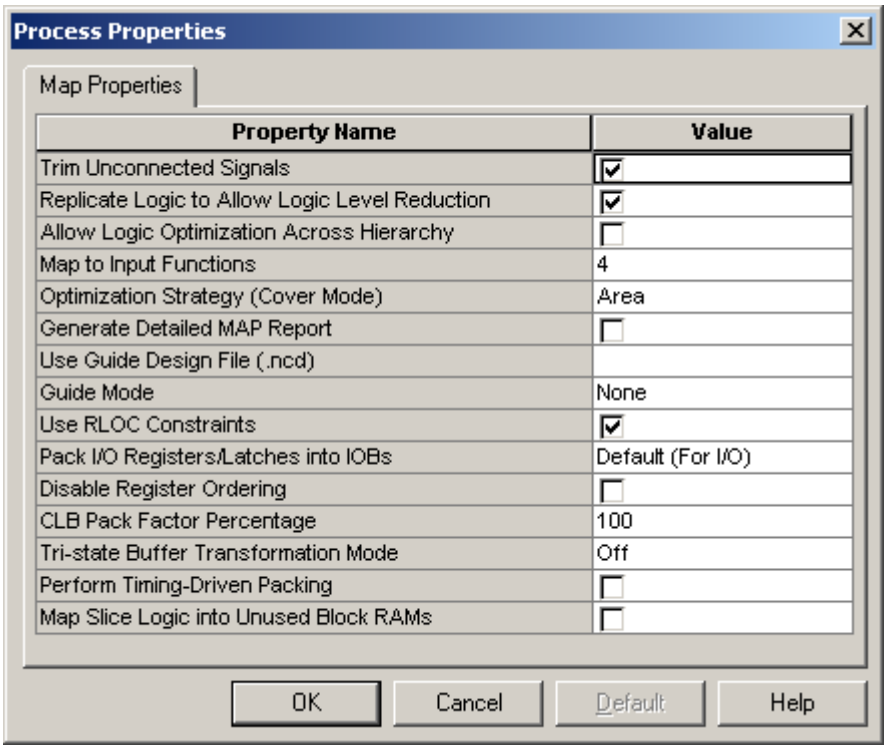


Click on the ‘OK’ button at the bottom of the window to apply the new settings.

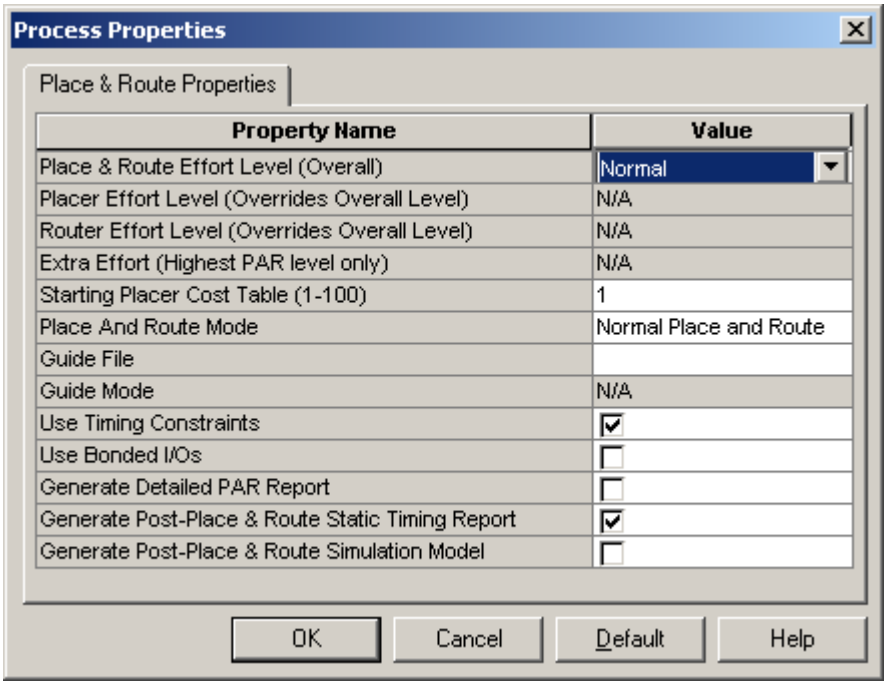
Next the Translate Properties must be checked. With the file ‘top.vhd’ still highlighted in the Module View right click on ‘Translate’ in the Process View. Select ‘Properties…’ to open the following window. Tick the item ‘Allow Unmatched LOC Constraints’, check all other settings match, and click ‘OK’.



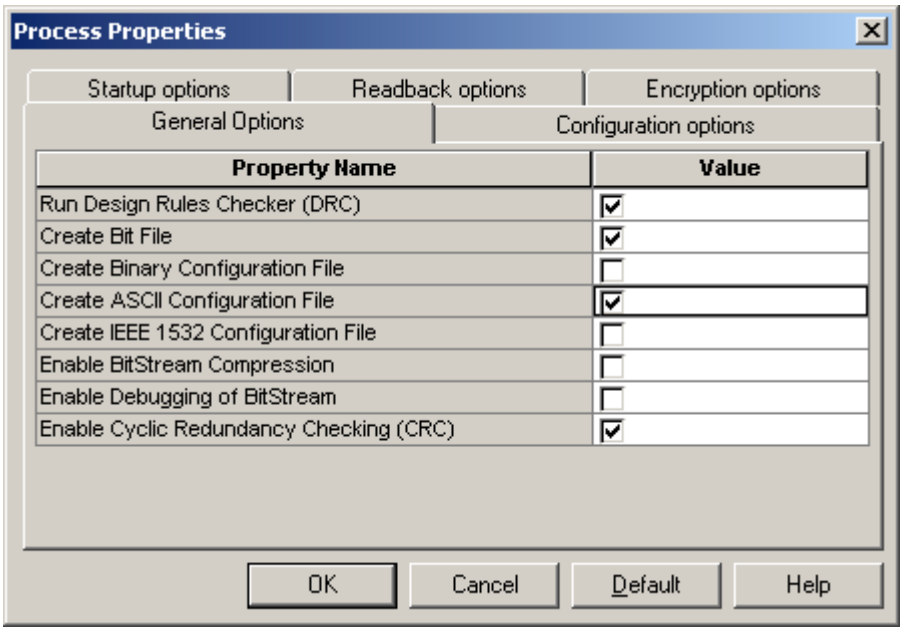
Next open the Process Properties window for the Map process. Check that the settings match those in the picture below.



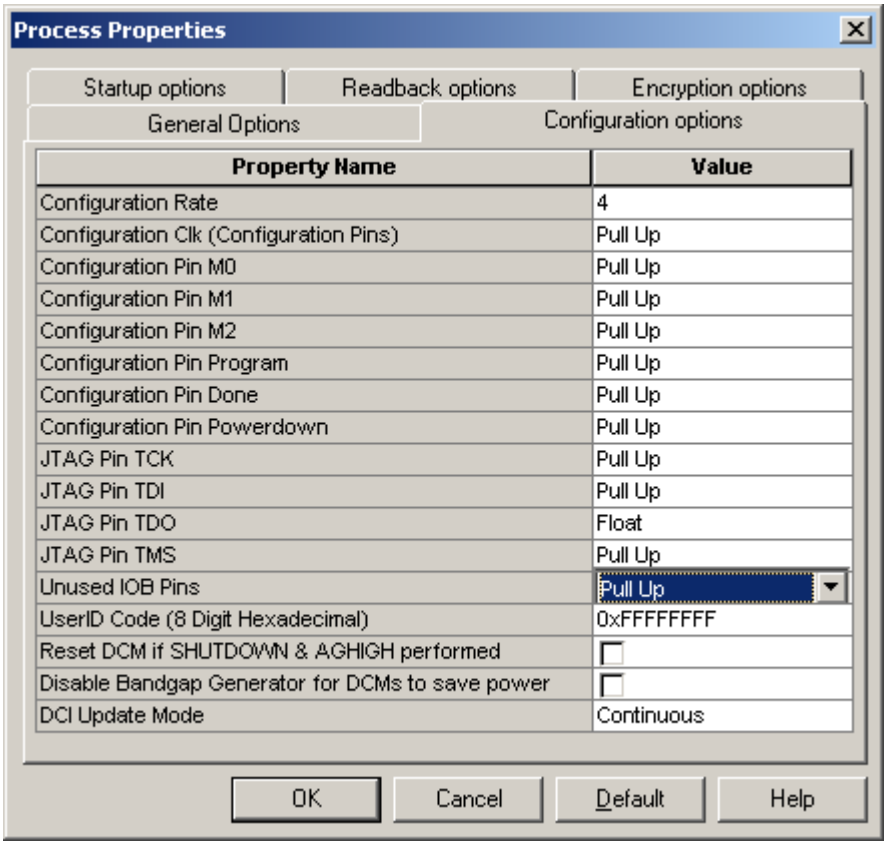
Next check the Place and Route process properties. For Example1 the 'Place & Route Effort Level (Overall)' typically needs to be set to 'Normal'. Make this change and check all other settings match the picture below and click 'OK'.



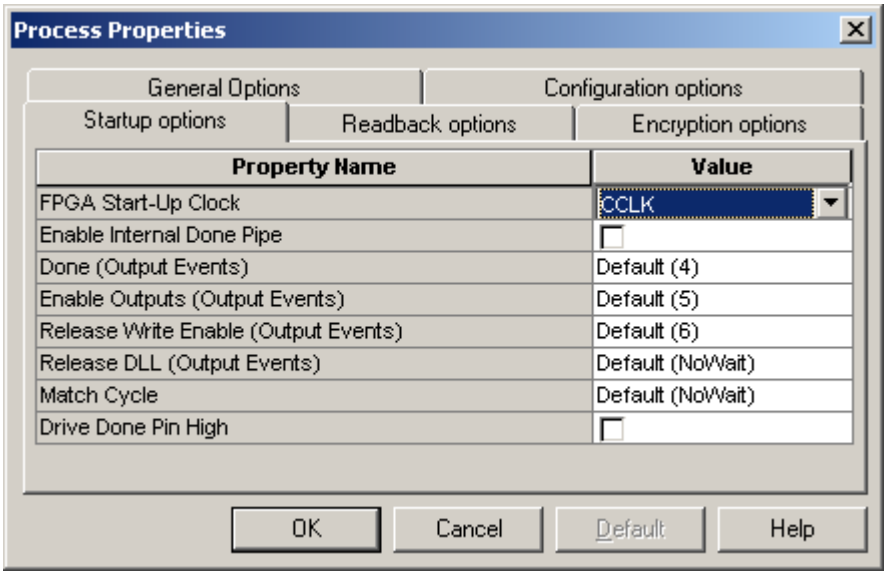
Next check the 'Generate Programming File' properties. With the 'General Options' tab at the front, tick the 'Create ASCII Configuration File' and then check that all other settings match for this tab.



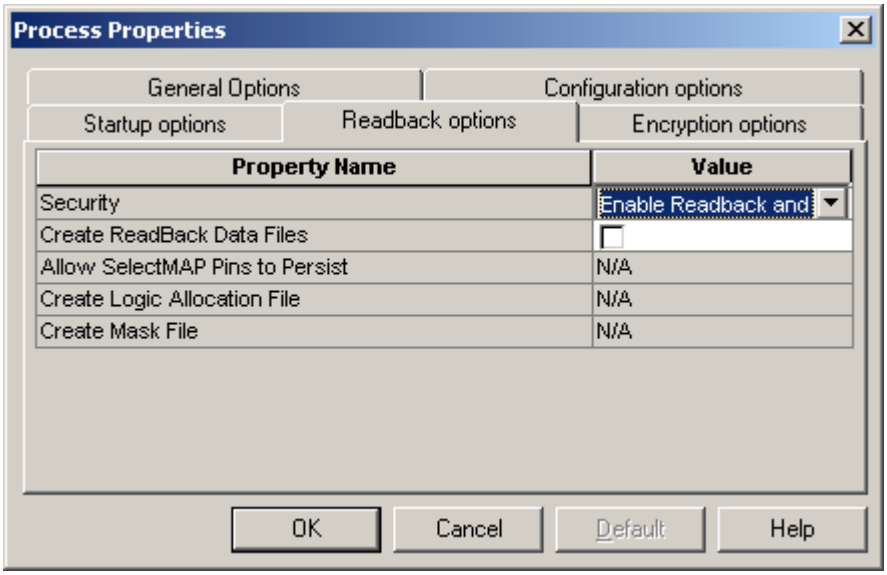
Bring the Configuration Options to the front. Select ‘Pull Up’ for the ‘Unused IOB Pins’ item. With this done check the settings match those shown in the picture below.



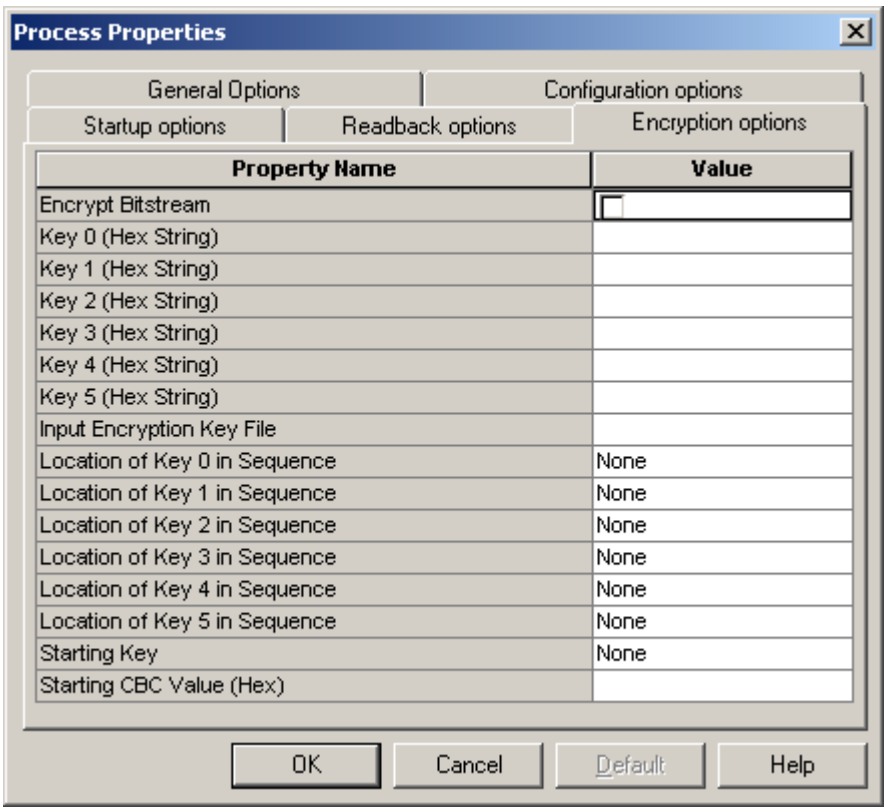
Next check the settings for the ‘Startup Options’ tab against those shown in the picture below.



Next check the ‘Readback Options’ against the picture below.



Finally check the ‘Encryption Options’ tab against the picture shown below.



When all tabs have been checked, click ‘OK’ to enter the new settings.

Step 7: Building the Project

At this point the project is ready to be built. All of the required design files have been added to the project and the project build settings have been checked. Example1 should now build as far as bitstream generation without error.

Although each example project supplied on the HUNT ENGINEERING CD will differ from Example1, the process to create a new project for ISE 5 is the same. The routine described in this section can therefore be repeated for each of the standard examples provided on the CD.

For each FPGA module type, each project contained on the CD provides all of the required design elements to ensure correct operation on that chosen module type. These elements include a Hardware Interface Layer that is used to correctly control external devices, user constraints information to control design timing and pin location and example VHDL to provide a structured starting point.

For users of ISE 6 design tools this document must be followed in order to convert the newer project format used on the HUNT ENGINEERING CD to the correct ISE 6 format. This section describes how to build an ISE 6 project from scratch, using the design source provided on the CD. This process is necessary as the standard XILINX tool version has moved on from ISE 6 and XILINX provide no mechanism for converting post ISE 6 projects back to ISE 6.

This document uses Example1 as the starting point for the creation of a new project. It is important to start from one of the standard examples provided on the HUNT ENGINEERING CD as this give the correct starting point for FPGA development with your FPGA module.

Please note: if you are using this section in order to create a brand new project with functionality that does not match any of the standard CD examples, then you must still start from Example1. Once you have created a correct project based around Example1 you may then insert your own unique code into the User-Ap entity, removing all unwanted logic. When doing this, you will need to refer to the relevant information in the ‘Making your own FPGA design’ section of your FPGA User Manual.

Converting Example1 for your Module Type

The HUNT ENGINEERING CD provides support for many different FPGA module types. For each module there is always a standard Example1 project provided on the CD. This example is the 'Getting Started' example for each module type and should always be used as the first step in FPGA development.

This section describes how to convert Example1 for the HERON-FPGA5 as an example of the conversion process. Although the design source varies for each module type, the principles shown here are the same regardless of type.

Step 1: Copying Example1 from the HUNT ENGINEERING CD

The first step in the conversion process is to copy Example1 onto your local hard drive. Make a directory on your local drive in which to store Example1.

On the HUNT ENGINEERING CD, all FPGA examples are provided below the 'fpga' directory. The 'fpga' directory is divided into sub-directories that reflect the name of the module type. In this document, Example1 for the HERON-FPGA5 is to be converted, so the directory 'fpga/fpga5v1/' will contain the appropriate project information. Identify the appropriate CD directory according to your module type.

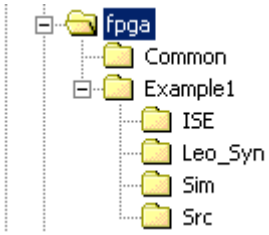
With the correct CD directory located you will need to copy Example 1 to your local drive. This can be done in one of two ways. The first method is to copy the Example 1 project by hand for the module type you are using. The second method is to unzip the ZIP file for that module type onto your hard drive.

When using the first approach you will need to copy the 'Common' directory and 'Example1' directory from the CD to a chosen directory on your local drive. The 'Example1' directory contains all design source that forms Example1 and the 'Common' directory provides design source common to all designs made for that module.

Please note, when copying files from your CD by hand you may need to edit the file attributes after copying. This is because on some operating systems Read-Only files on the CD will become Read-Only files on your local drive. All files in the 'Example1' directory should be set to Read-Write while all files in the 'Common' directory must remain Read-Only.

When using the second approach you will be unzipping all examples for that module, including Example1. When unzipping all project examples, the read-write attributes will automatically be set correctly.

The picture below shows a new directory on the local drive named 'fpga'. In the 'fpga' directory are the copied 'Common' and 'Example1' directories.



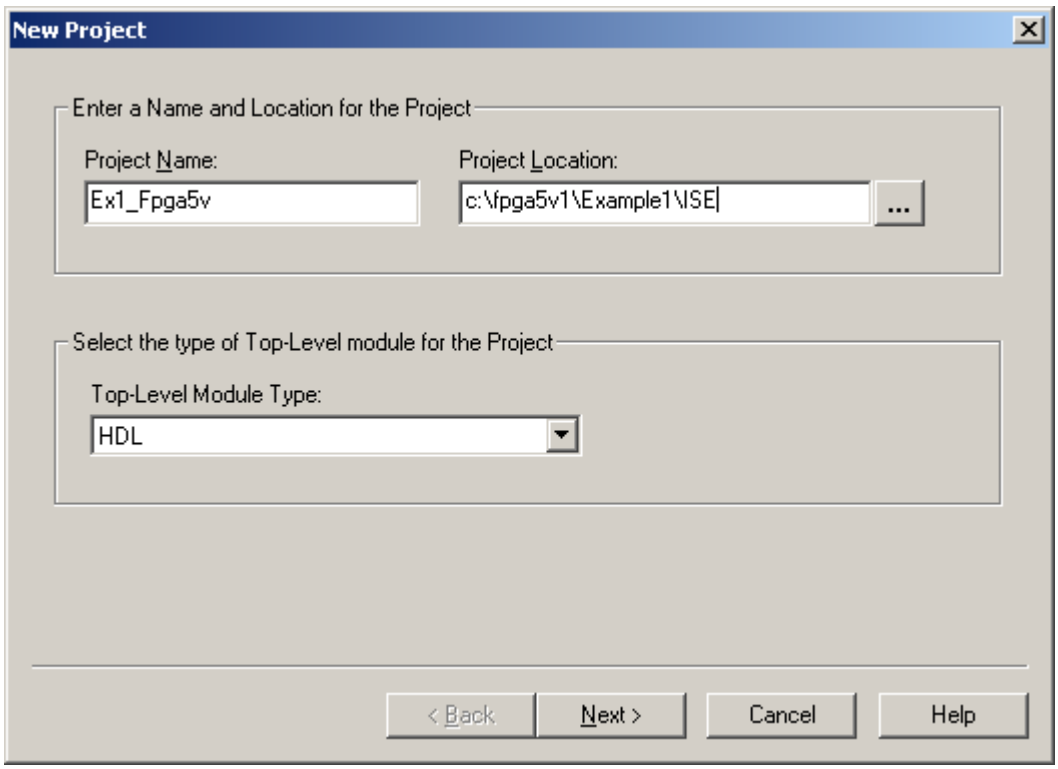
Step 2: Creating a New Project File

With the Example1 example directory and Common directory copied onto your Local Drive you can now begin building an ISE 6 project.

Open the ISE 6 Project Navigator if it is not already open. Please note, in the remainder of this section an example conversion is shown for Example 1 for the HERON-FPGA5 where this conversion is performed in ISE 6.2. If you are using a different ISE 6 version then although the windows shown may not perfectly match, the conversion process is still the same.

Next, delete the project file for the Example1 project in the new directory you have created on your local drive. The project file will be located in the 'ISE' sub-directory of the 'Example1' directory and will have the extension '.ise'. This existing project file must be removed as it will not be useable in ISE 6 and must be replaced with an appropriately constructed project file.

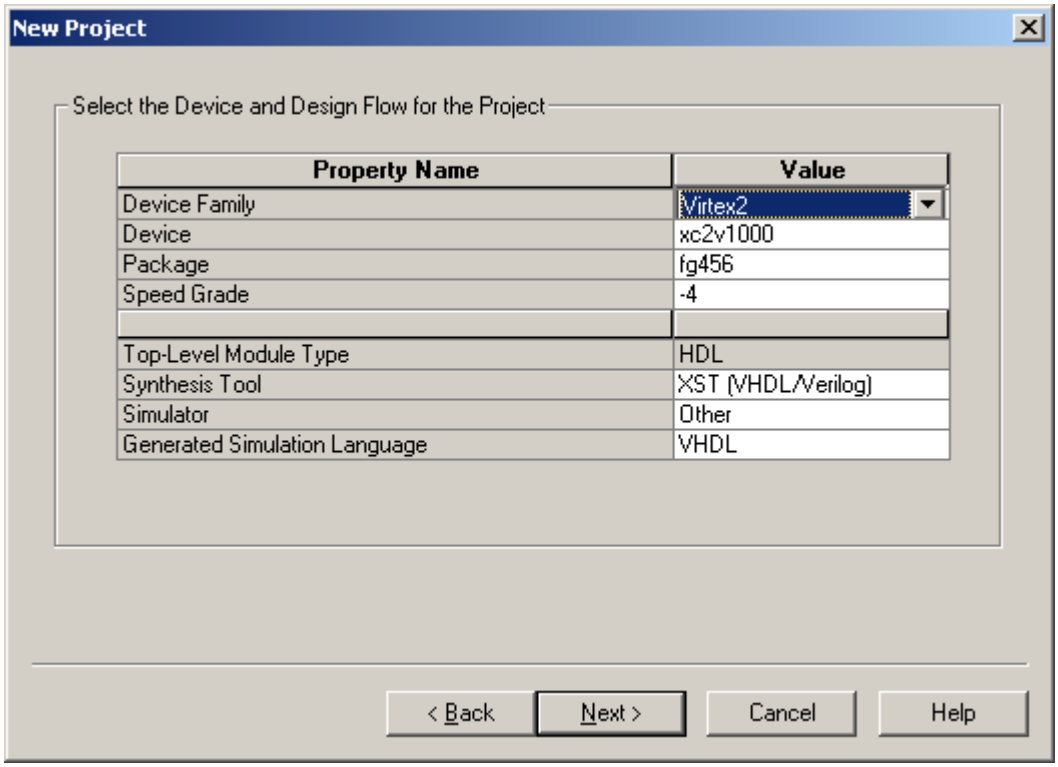
With the existing file deleted, select the menu item 'File→New Project…' to begin creating a new project. The following window should be displayed.



Enter the correct project name in the 'Project Name' field. For Example1 this should be set to be the same project name as the Example1 project file on the HUNT ENGINEERING CD (minus the .ise extension).

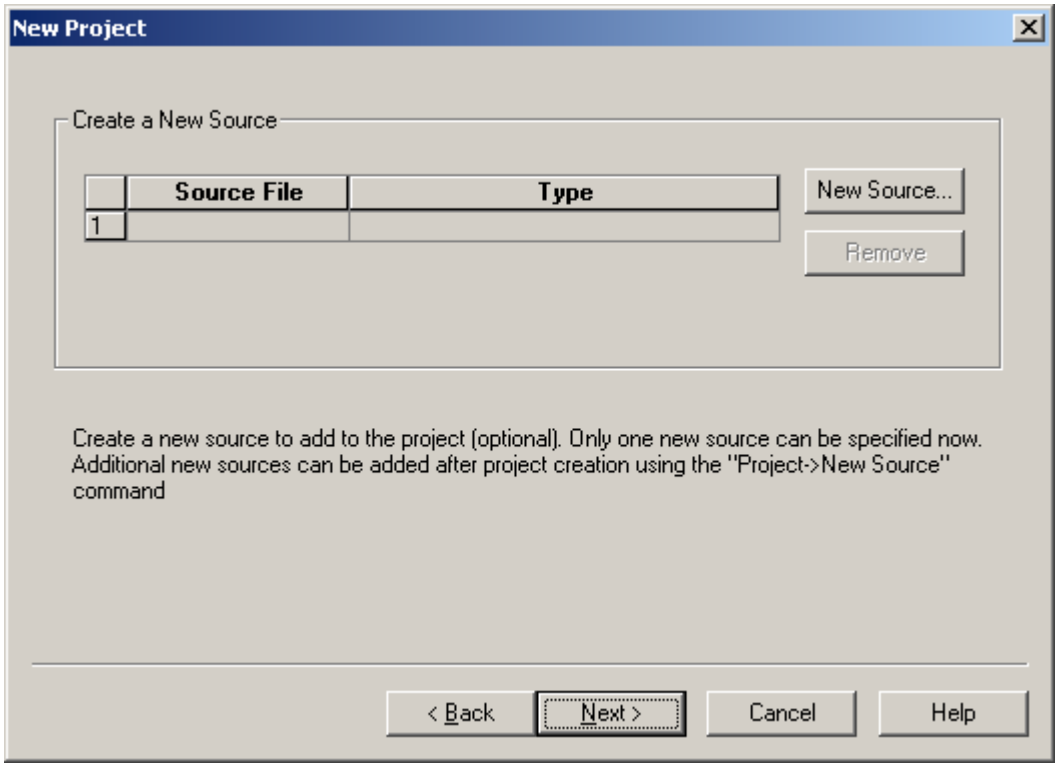
Next, enter the correct location into the 'Project Location' field. This field should match the location of the 'Example1/ISE' directory you have made on your local drive. Next, ensure the 'Top-Level Module Type' field is set to HDL.

With these steps completed click on the ‘Next >’ button at the bottom of the window, to display the following:

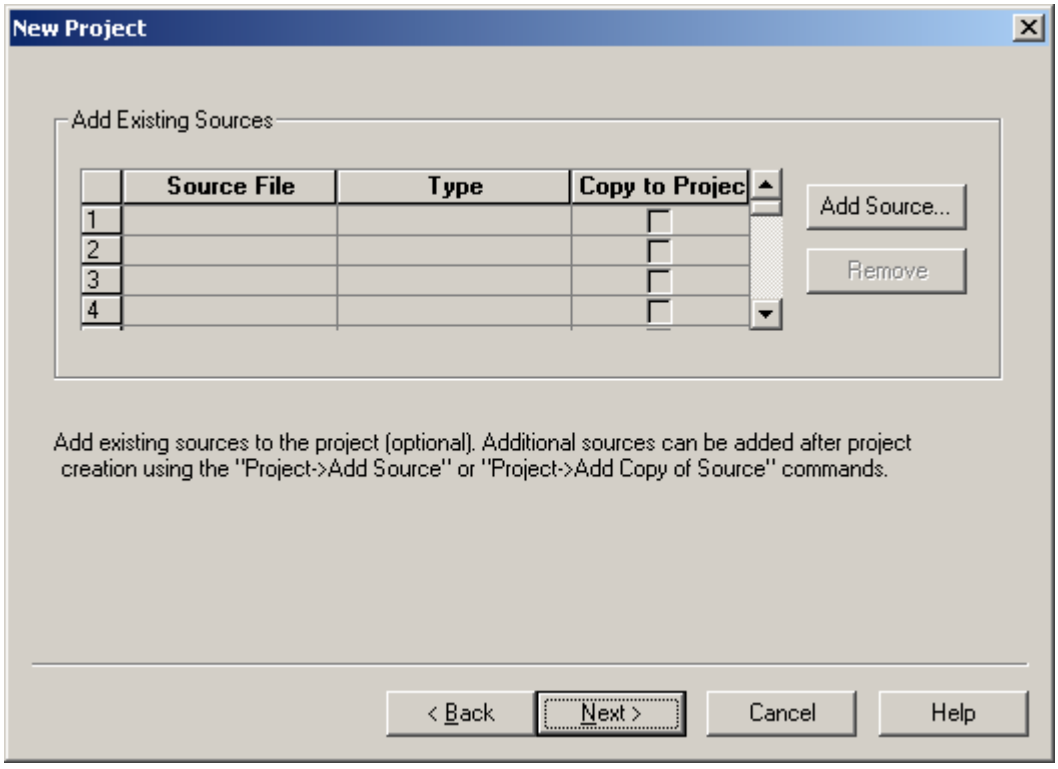


Fill out the appropriate device information according to the module type you are using. If you are unsure of the correct information refer to the User Manual for that module type. When you have done this click the ‘Next >’ button.

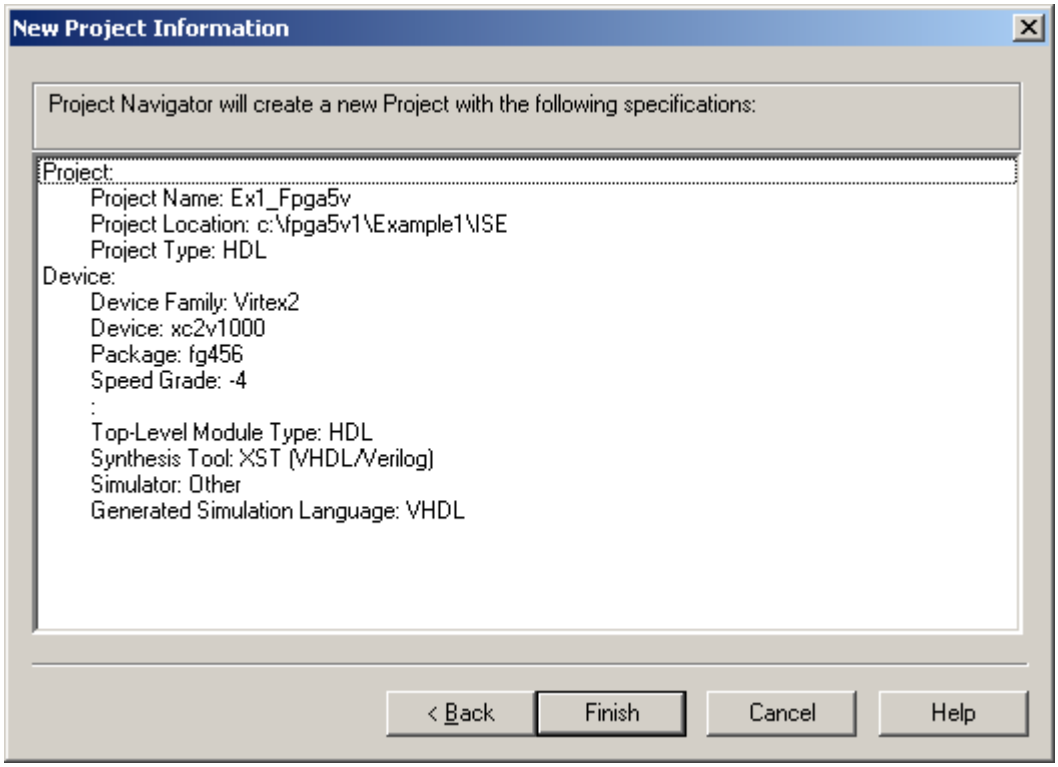
The following window will then be displayed. Simply click ‘Next >’.



The following window will then be displayed. Again, click ‘Next >’.



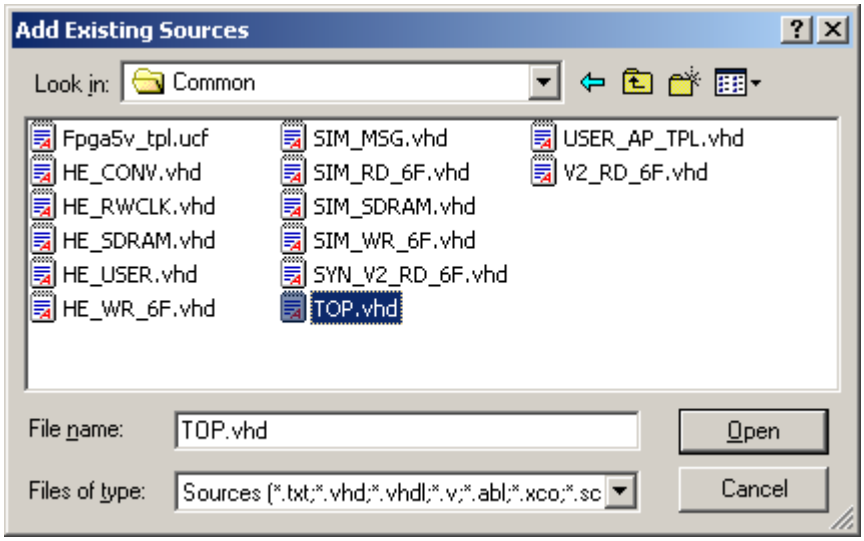
Finally, the following window is displayed providing a summary of all the project information you have entered. Click ‘Finish’ to make the new project file.



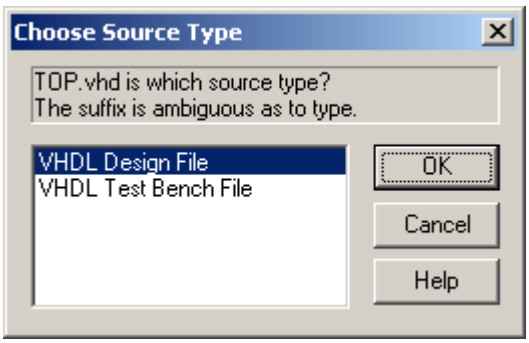
Step 3: Adding VHDL Source to the New Project

The next step is to add design source, starting with the top level of the hierarchy. For all FPGA module projects the top level of the design is always contained in the file 'top.vhd'. 'top.vhd' is always provided as part of the 'Common' directory for each module type.

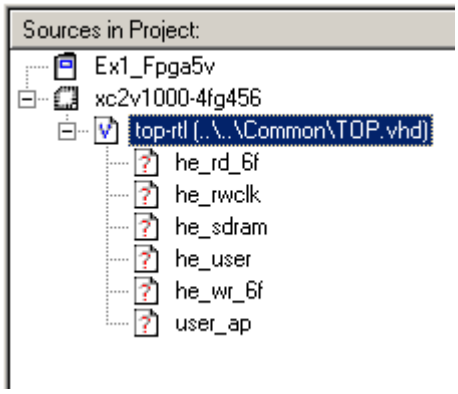
Select the menu item 'Project→Add Source…'. The following window will be displayed where you will need to navigate to the 'Common' directory that was created on your local drive. Select the file 'top.vhd' and click 'Open'.



The following window will then appear. Select 'VHDL Design File' and click OK to add 'top.vhd' to the project.



With this done, the Module View window will now look similar to the picture below, depending on the particular source files that are required by the module type you are using:

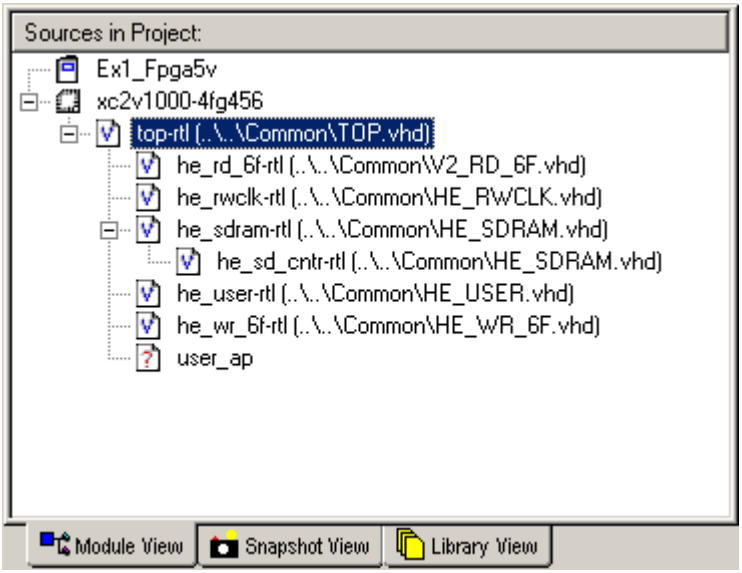


In the case of the FPGA5v1 example conversion, after adding 'top.vhd' we can now see 6 more design entities are needed. One of these entities is the User-Application level of the design which contains the VHDL that makes this example the getting started example, Example1. The other entities shown are part of the Hardware Interface Layer and are found in the 'Common' directory.

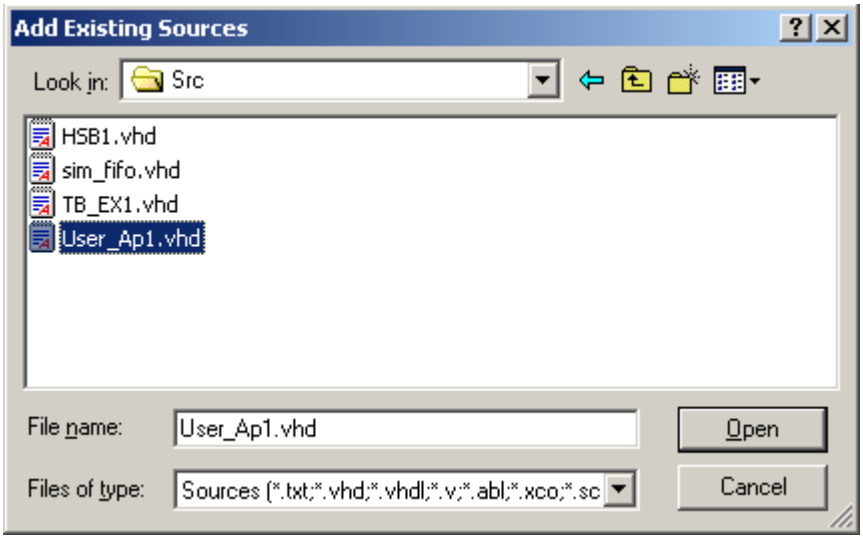
First add the appropriate files from the 'Common' directory in order to replace the red question mark icons with correct entities. To do this, you will again need to use the 'Add Source…' menu item. Navigate to the 'Common' directory and select the files that have names that match the entities in the Module View of your new project.

Please note: the HE_RD_6F entity is provided in the 'Common' directory in the source file 'V2_RD_6F'.

When adding each file, the correct Source Type will be 'VHDL Design File' as was selected when adding 'top.vhd'. When you have added all required Hardware Interface Layer components the Module View should look similar to the picture below for the FPGA5v1 conversion:



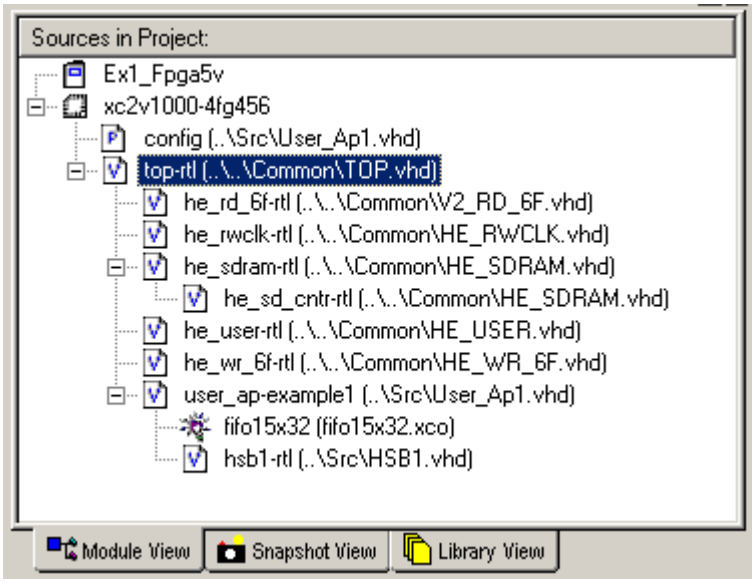
Next you will need to navigate to the 'Src' directory of Example1 and add the User_Ap file to the project:



After the 'user_ap' entity has been added to the project you will see which other source files are required below this entity. Add the appropriate source files from the 'Src' directory.

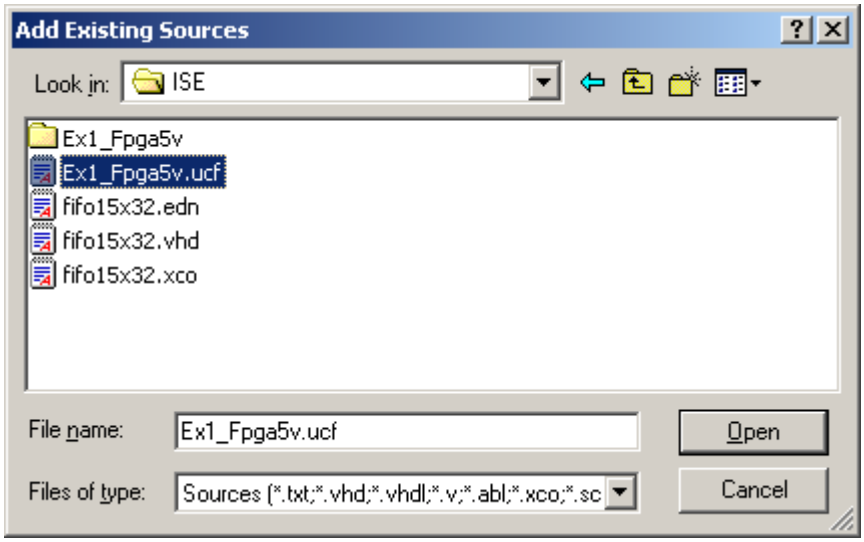
After you have added all of required VHDL source files from the 'Src' directory there may still be red question marks against entities in the hierarchy. These entities will correspond to Core Gen components that are placed in the Example1 'ISE' directory. In the case of Example1 there is one Core Gen component called 'fifo15x32' that must be added to the project from the 'ISE' directory.

With all relevant VHDL source added to the project the Module View should look similar to the picture shown below for the FPGA5v1 conversion:

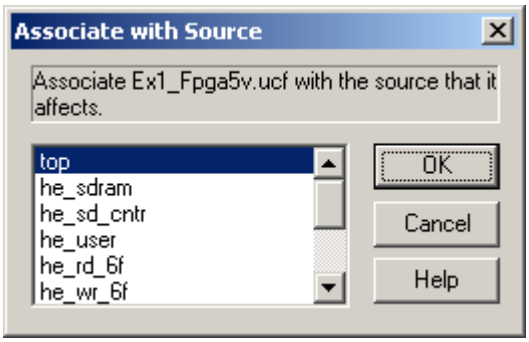


Step 4: Adding User Constraints

The next step is to add user design constraints to the project. Using 'Project→Add Source…' add the user constraints file contained in the 'ISE' directory of the project.

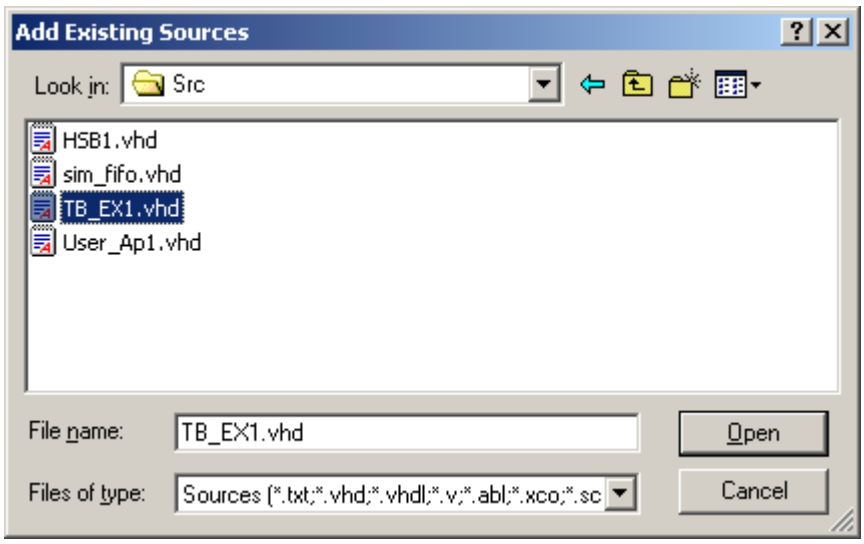


Select the UCF file and click 'Open'. The following window will appear to allow you to specify the design file to which the user constraints should be associated. Highlight 'top' and click 'OK'.

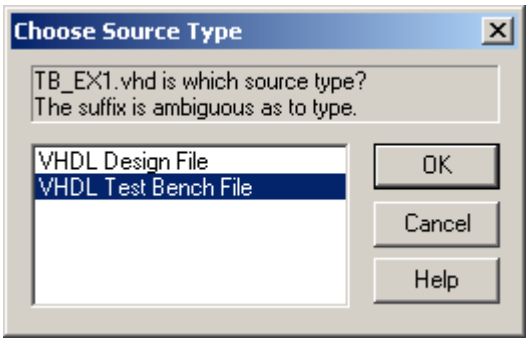


Step 5: Adding a Simulation Test-Bench

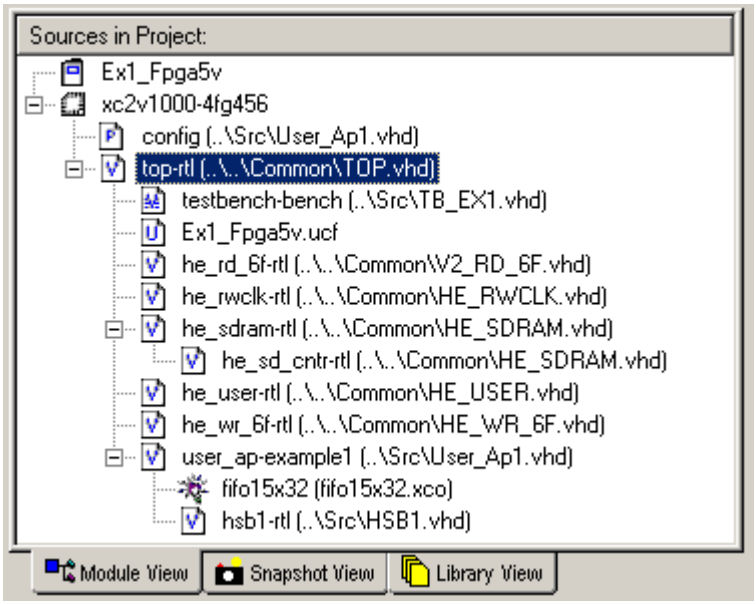
Typically, a project will also include a test-bench for simulation. For Example1 there is a test-bench provided in the 'Src' directory of the project. This file must also be added to the project using 'Project→Add Source…'. Navigate to the 'Src' directory, highlight the file that beings 'TB_' and click 'Open'.



The following window will appear where you need to specify the source type. Select 'VHDL Test Bench File' and click 'OK'.



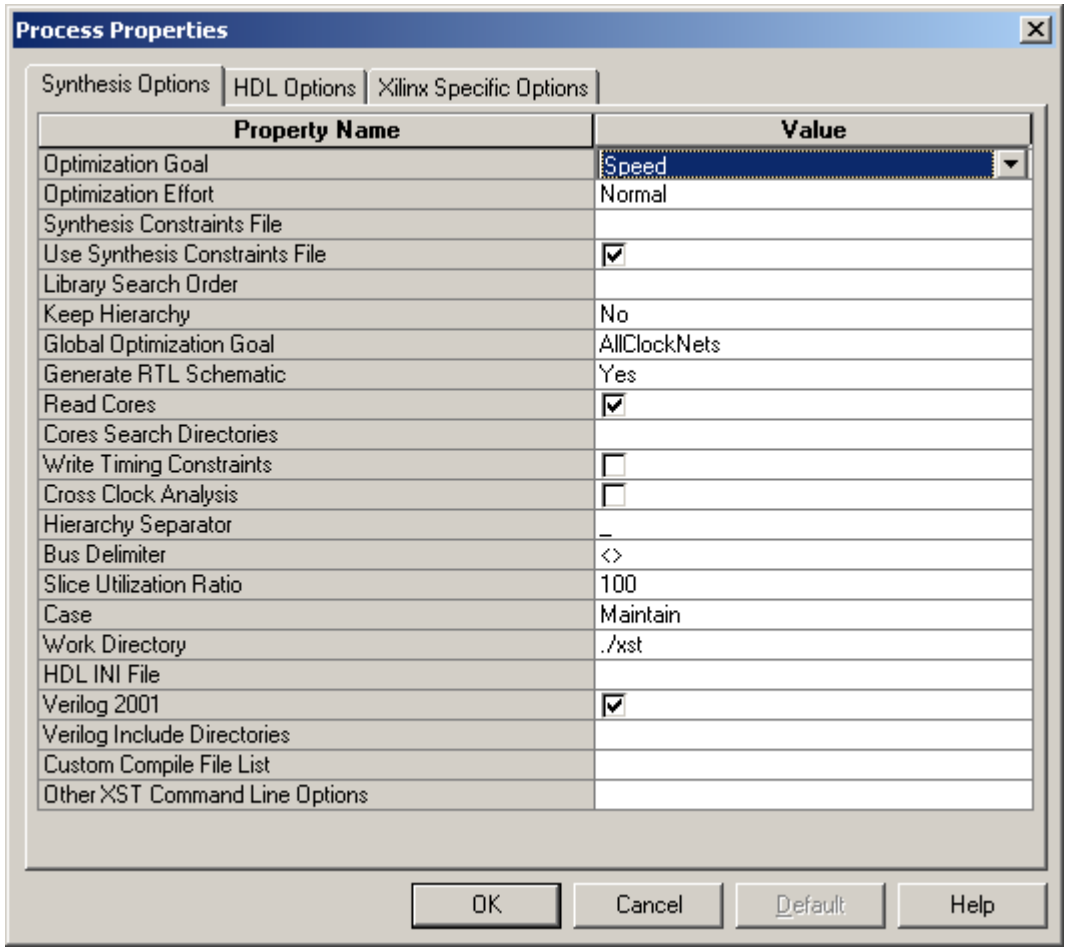
At this point the Module View should look similar to the picture shown below for the FPGA5v1 conversion process.



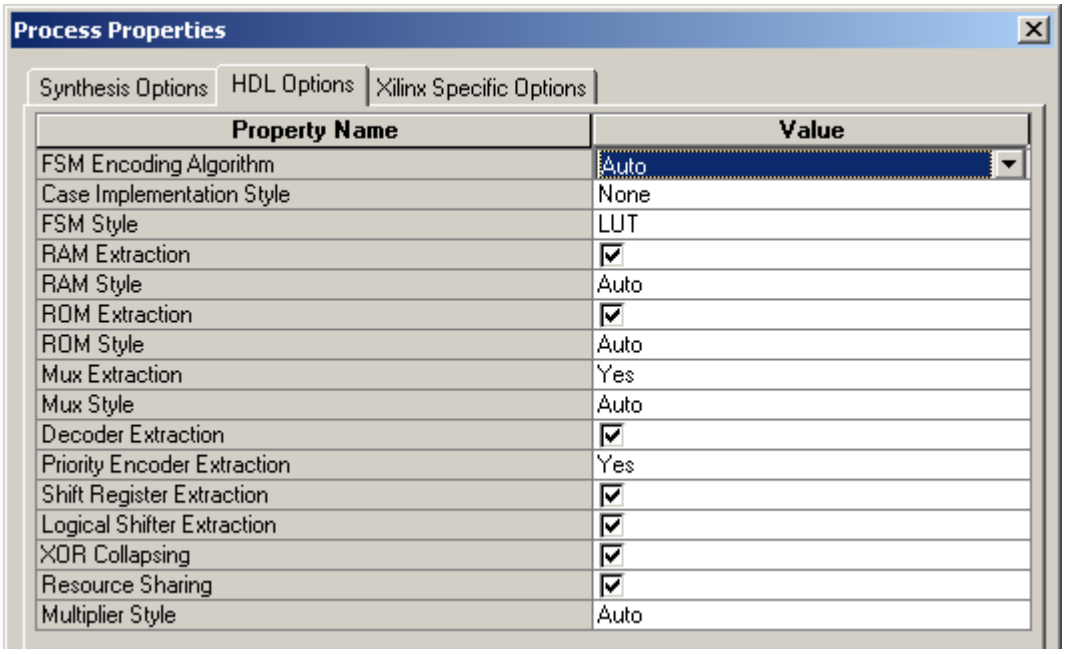
Step 6: Setting Project Build Options

The last step in creating a new project is to apply the necessary project settings that will allow the design to be built correctly.

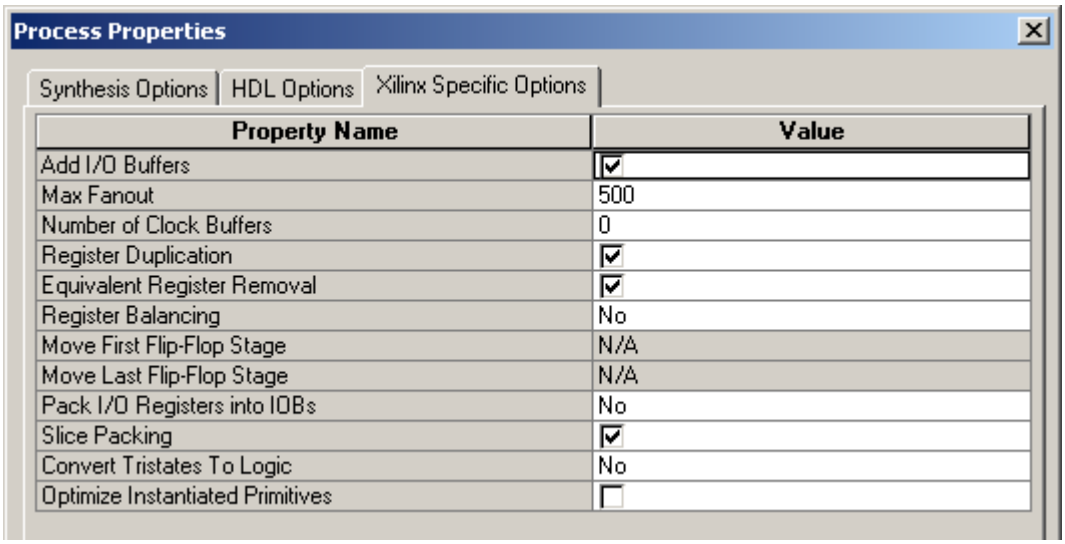
Ensure the file 'top.vhd' is highlighted in the Module View, and then right click on 'Synthesize' in the Process View. Select 'Properties…' to open the following window. With the 'Synthesis Options' tab at the front, check that the settings match those shown below.



Next bring the ‘HDL Options’ tab to the front and check that the settings match those in the picture below.

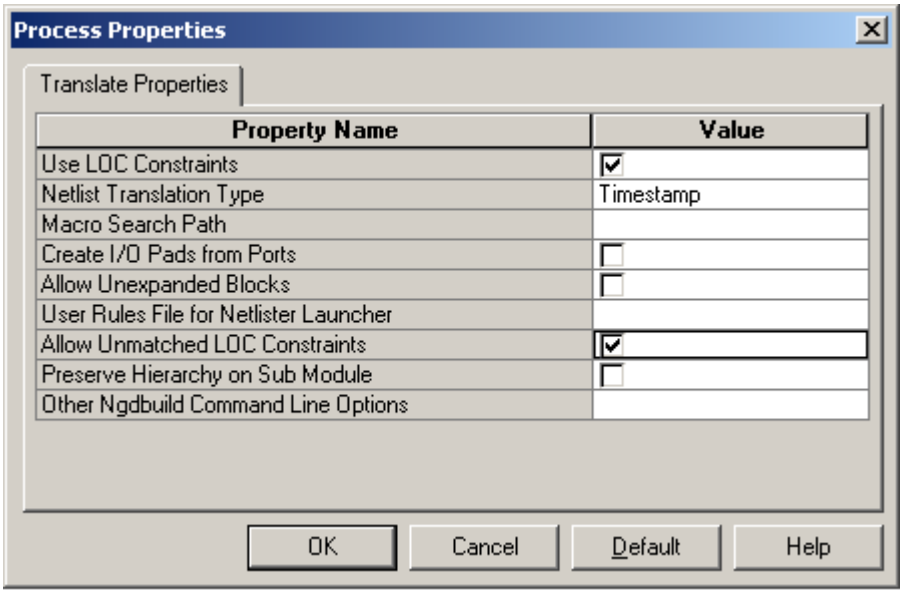


Next bring the ‘Xilinx Specific Options’ tab to the front. Change the ‘Number of Clock Buffers’ item to ‘0’, and set the ‘Pack I/O Registers into IOBs’ item to ‘No’. With this done, check that the settings match those in the picture below.

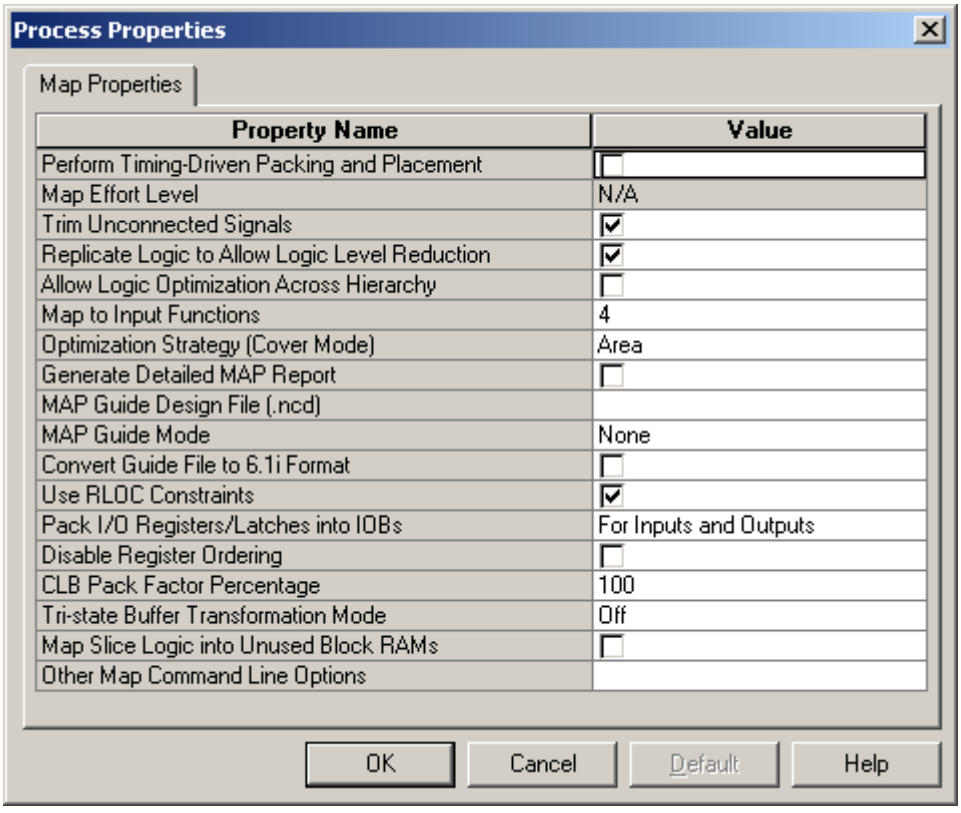


Click on the ‘OK’ button at the bottom of the window to apply the new settings.

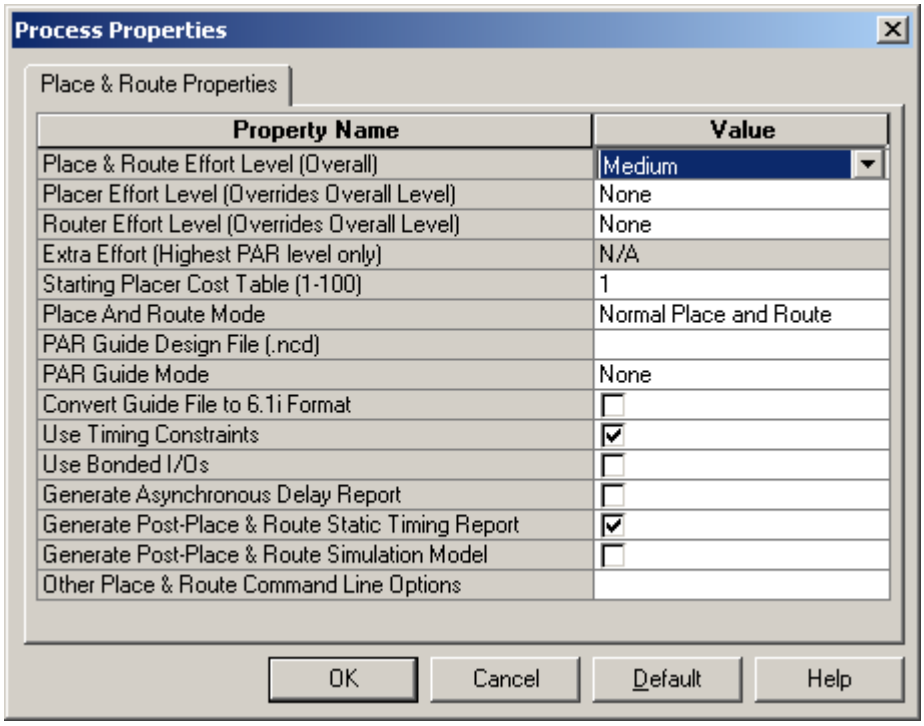
Next the Translate Properties must be checked. With the file 'top.vhd' still highlighted in the Module View right click on 'Translate' in the Process View. Select 'Properties…' to open the following window. Tick the item 'Allow Unmatched LOC Constraints', check all other settings match, and click 'OK'.



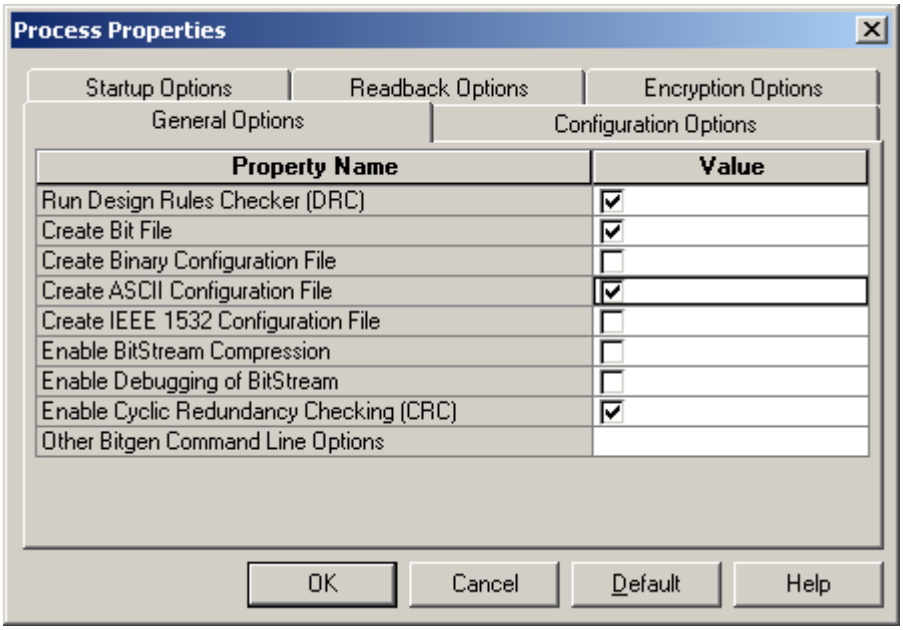
Next open the Process Properties window for the Map process. Check that the settings match those in the picture below.



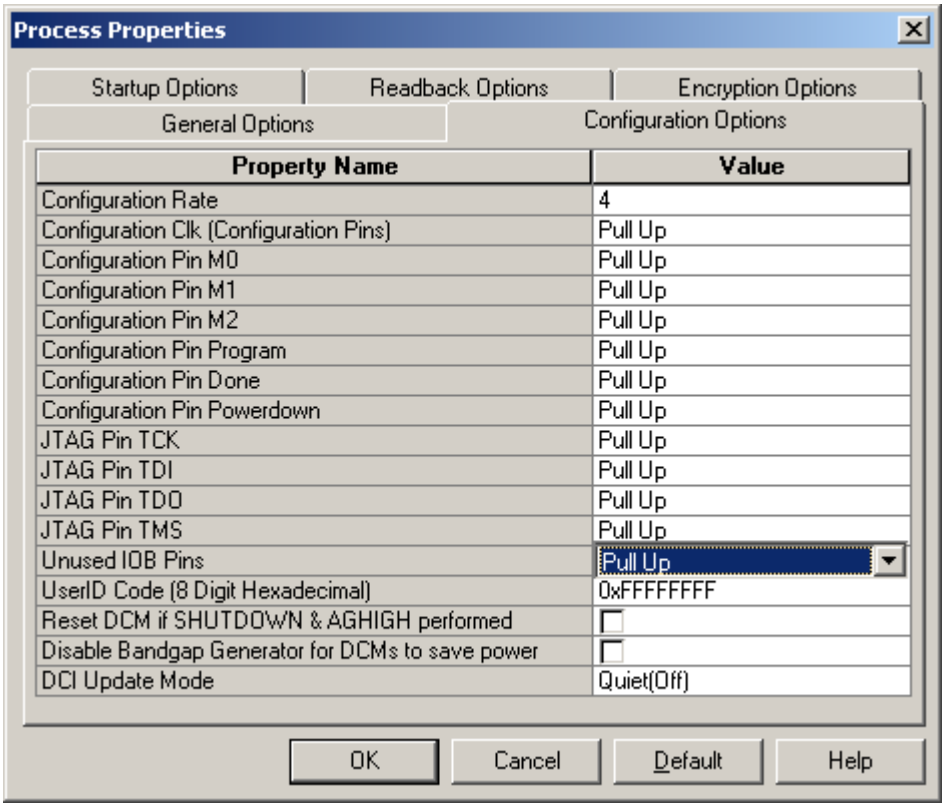
Next check the Place and Route process properties. For Example1 the 'Place & Route Effort Level (Overall)' typically needs to be set to 'Medium'. Make this change and check all other settings match the picture below and click 'OK'.



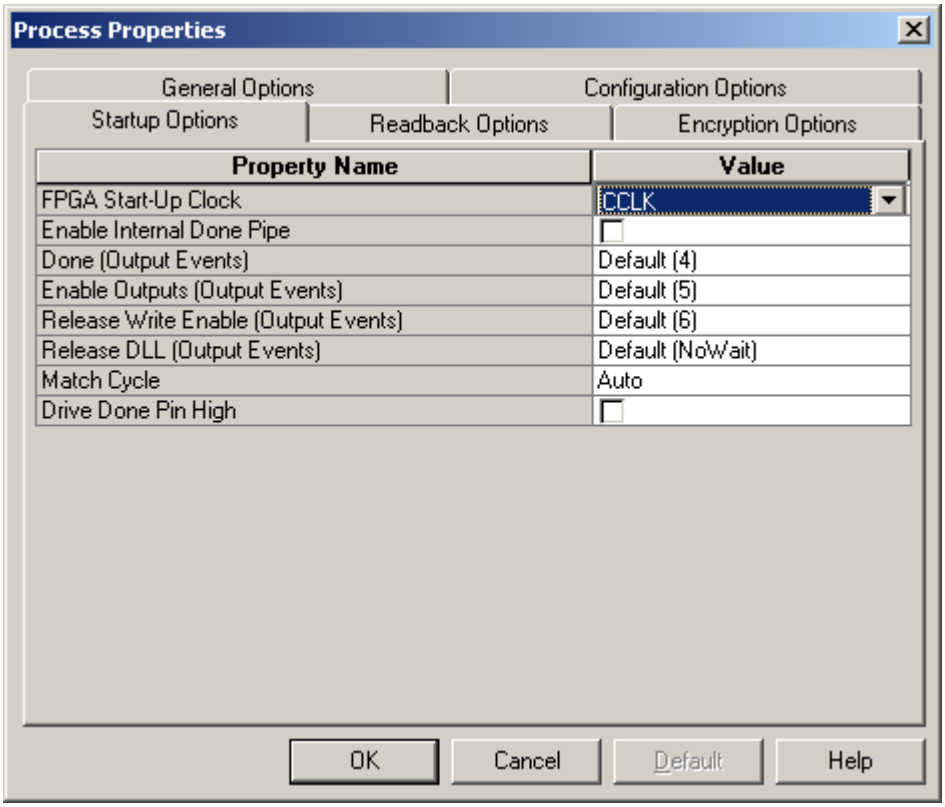
Next check the 'Generate Programming File' properties. With the 'General Options' tab at the front, tick the 'Create ASCII Configuration File' and then check that all other settings match for this tab.



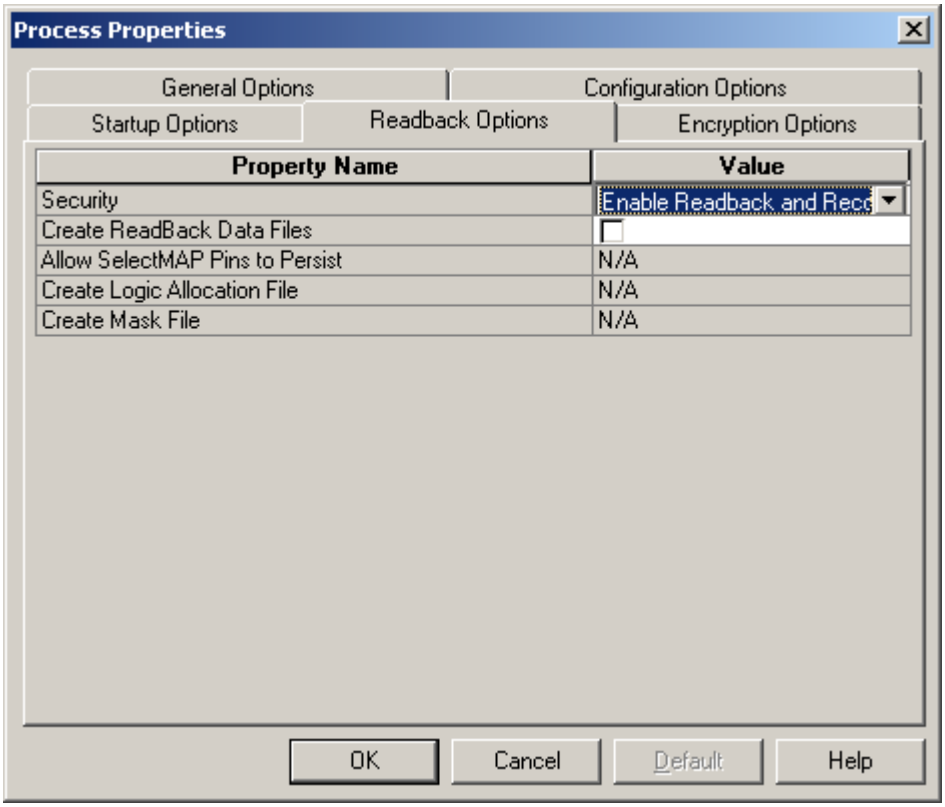
Bring the Configuration Options to the front. Select ‘Pull Up’ for the ‘Unused IOB Pins’ item. With this done check the settings match those shown in the picture below.



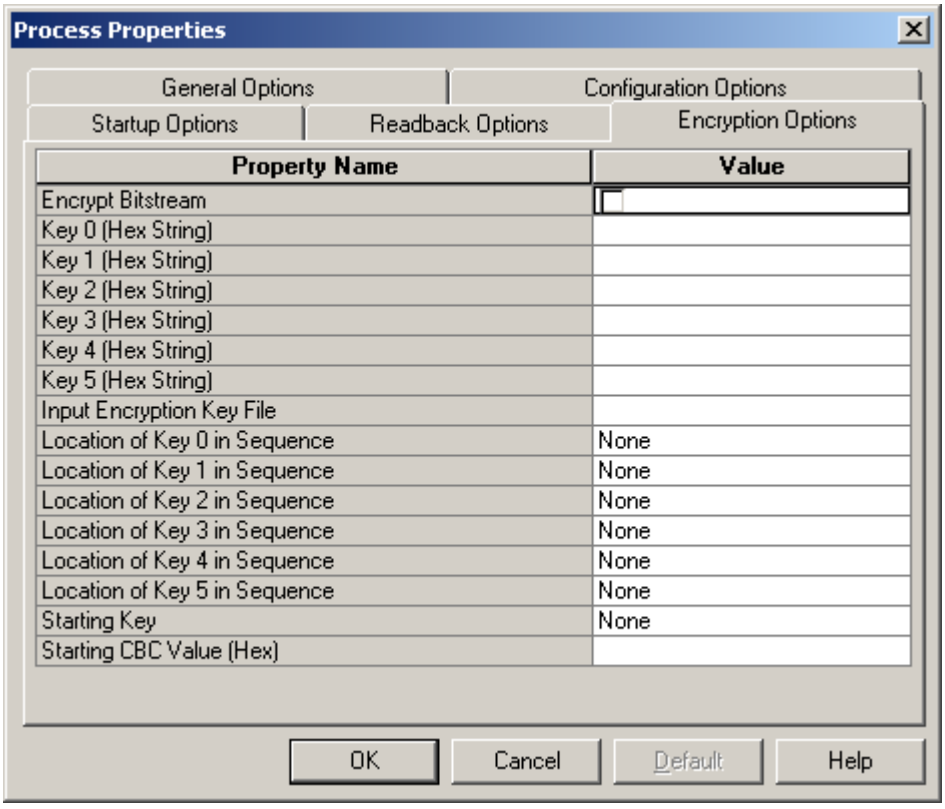
Next check the settings for the ‘Startup Options’ tab against those shown in the picture below.



Next check the ‘Readback Options’ against the picture below.



Finally check the ‘Encryption Options’ tab against the picture shown below.



When all tabs have been checked, click ‘OK’ to enter the new settings.

Step 7: Building the Project

At this point the project is ready to be built. All of the required design files have been added to the project and the project build settings have been checked. Example1 should now build as far as bitstream generation without error.

Although each example project supplied on the HUNT ENGINEERING CD will differ from Example1, the process to create a new project for ISE 6 is the same. The routine described in this section can therefore be repeated for each of the standard examples provided on the CD.

For each FPGA module type, each project contained on the CD provides all of the required design elements to ensure correct operation on that chosen module type. These elements include a Hardware Interface Layer that is used to correctly control external devices, user constraints information to control design timing and pin location and example VHDL to provide a structured starting point.

This section describes how to build an ISE 7.1 project from scratch, using the design source provided on the CD.

This document uses Example1 as the starting point for the creation of a new project. It is important to start from one of the standard examples provided on the HUNT ENGINEERING CD as this give the correct starting point for FPGA development with your FPGA module.

Please note: if you are using this section in order to create a brand new project with functionality that does not match any of the standard CD examples, then you must still start from Example1. Once you have created a correct project based around Example1 you may then insert your own unique code into the User-Ap entity, removing all unwanted logic. When doing this, you will need to refer to the relevant information in the 'Making your own FPGA design' section of your FPGA User Manual.

Converting Example1 for your Module Type

The HUNT ENGINEERING CD provides support for many different FPGA module types. For each module there is always a standard Example1 project provided on the CD. This example is the 'Getting Started' example for each module type and should always be used as the first step in FPGA development.

This section describes how to convert Example1 for the HERON-FPGA5 as an example of the conversion process. Although the design source varies for each module type, the principles shown here are the same regardless of type.

Step 1: Copying Example1 from the HUNT ENGINEERING CD

The first step in the conversion process is to copy Example1 onto your local hard drive. Make a directory on your local drive in which to store Example1.

On the HUNT ENGINEERING CD, all FPGA examples are provided below the 'fpga' directory. The 'fpga' directory is divided into sub-directories that reflect the name of the module type. In this document, Example1 for the HERON-FPGA5 is to be converted, so the directory 'fpga/fpga5v1/' will contain the appropriate project information. Identify the appropriate CD directory according to your module type.

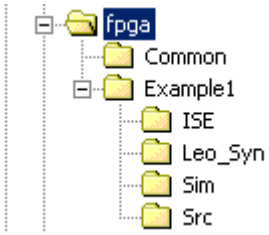
With the correct CD directory located you will need to copy Example 1 to your local drive. This can be done in one of two ways. The first method is to copy the Example 1 project by hand for the module type you are using. The second method is to unzip the ZIP file for that module type onto your hard drive.

When using the first approach you will need to copy the 'Common' directory and 'Example1' directory from the CD to a chosen directory on your local drive. The 'Example1' directory contains all design source that forms Example1 and the 'Common' directory provides design source common to all designs made for that module.

Please note, when copying files from your CD by hand you may need to edit the file attributes after copying. This is because on some operating systems Read-Only files on the CD will become Read-Only files on your local drive. All files in the 'Example1' directory should be set to Read-Write while all files in the 'Common' directory must remain Read-Only.

When using the second approach you will be unzipping all examples for that module, including Example1. When unzipping all project examples, the read-write attributes will automatically be set correctly.

The picture below shows a new directory on the local drive named 'fpga'. In the 'fpga' directory are the copied 'Common' and 'Example1' directories.



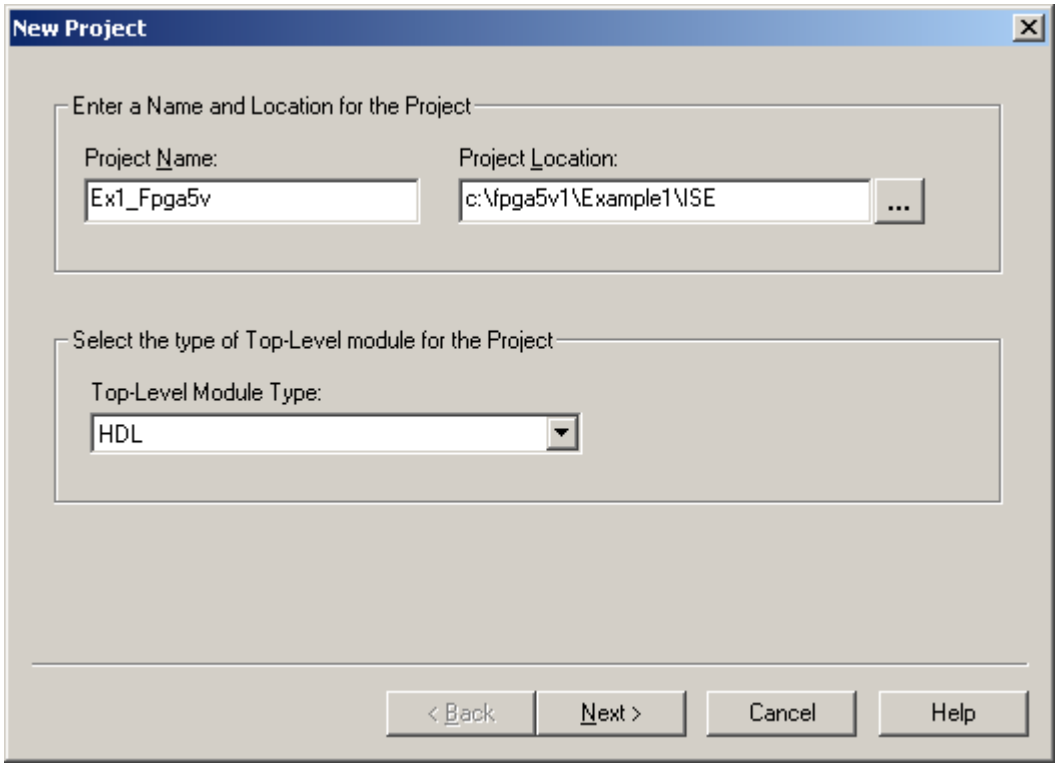
Step 2: Creating a New Project File

With the Example1 example directory and Common directory copied onto your Local Drive you can now begin building an ISE 7 project.

Open the ISE 7 Project Navigator if it is not already open. Please note, in the remainder of this section an example conversion is shown for Example 1 for the HERON-FPGA5 where this conversion is performed in ISE 7.1, with Service Pack 1 installed. If you are using a different ISE 7 version then although the windows shown may not perfectly match, the conversion process is still the same.

Next, delete the project file for the Example1 project in the new directory you have created on your local drive. This must be done, as we are about to create a new project file.

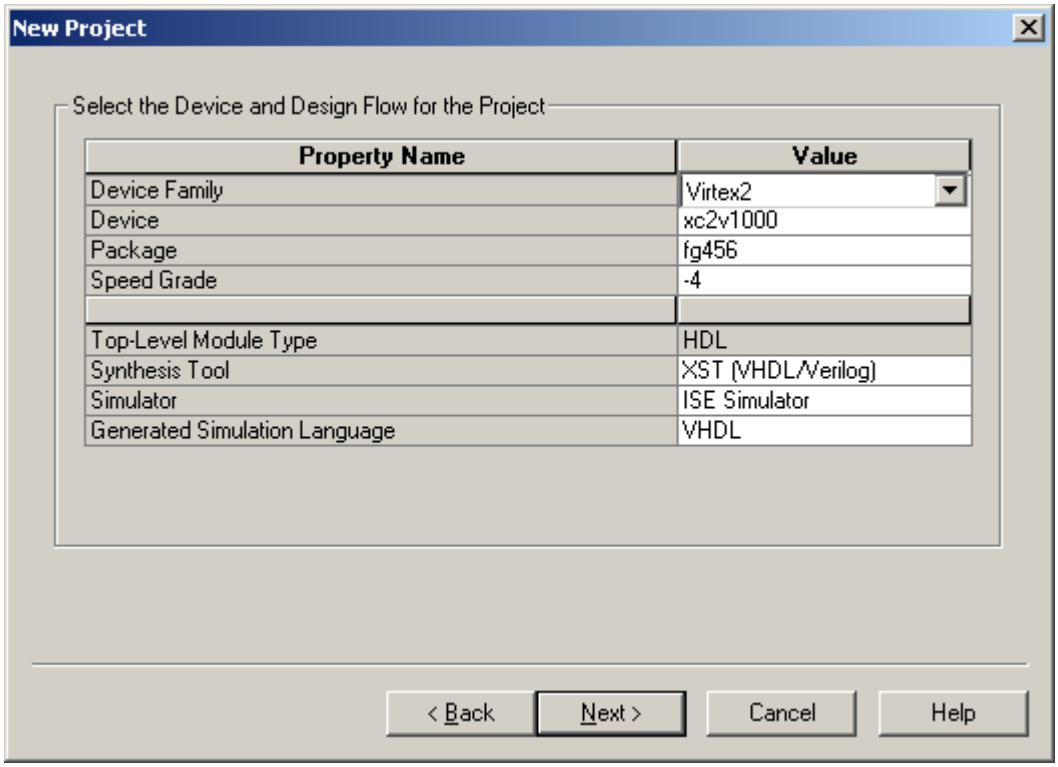
With the existing file deleted, select the menu item 'File→New Project…' to begin creating a new project. The following window should be displayed.



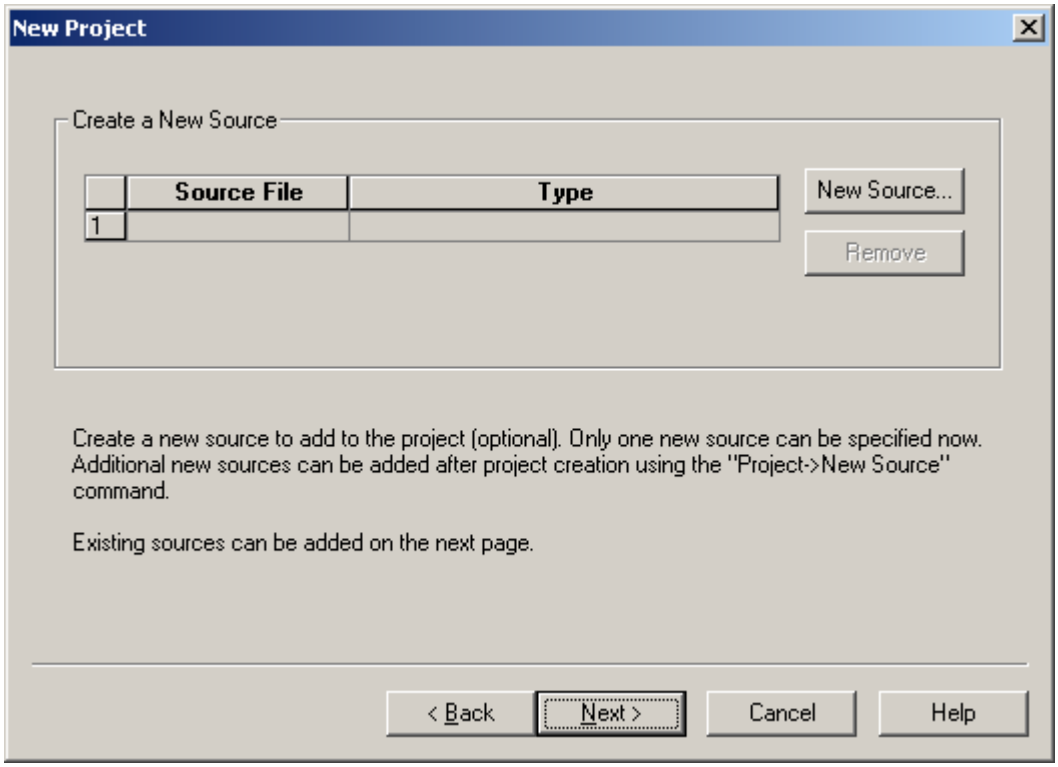
Enter the correct project name in the 'Project Name' field. For Example1 this should be set to be the same project name as the Example1 project file on the HUNT ENGINEERING CD (minus the .ise extension).

Next, enter the correct location into the 'Project Location' field. This field should match the location of the 'Example1/ISE' directory you have made on your local drive. Next, ensure the 'Top-Level Module Type' field is set to HDL.

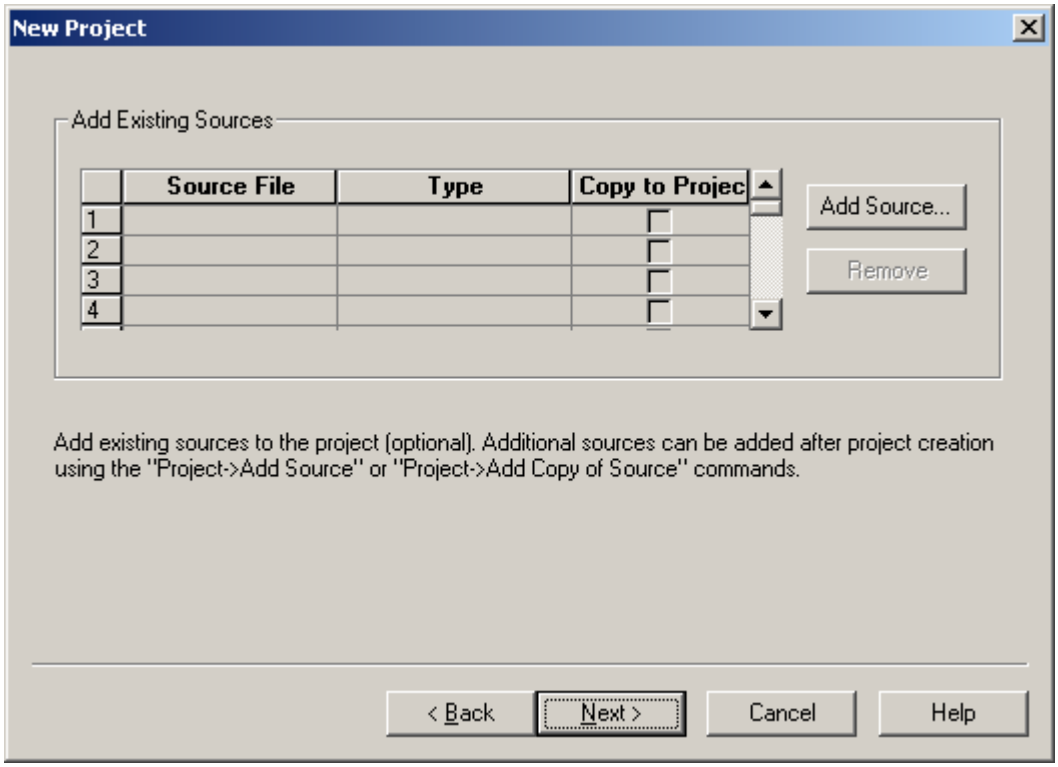
With these steps completed click on the ‘Next >’ button at the bottom of the window, to display the following:



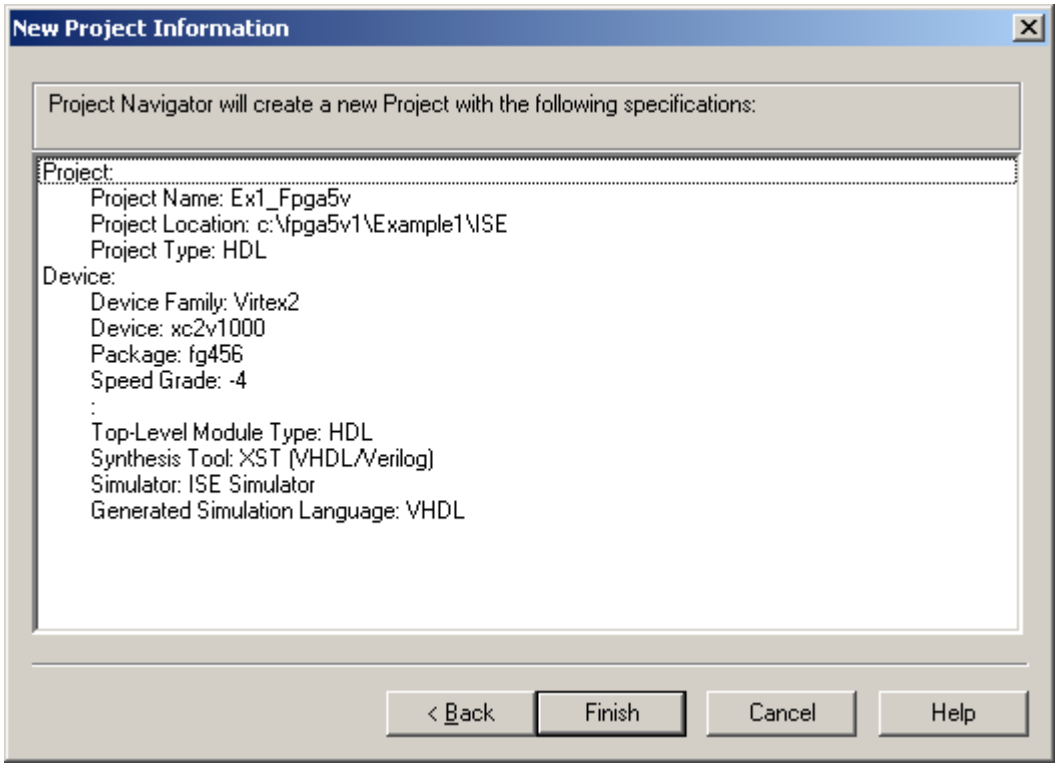
Fill out the appropriate device information according to the module type you are using. If you are unsure of the correct information refer to the User Manual for that module type. When you have done this click the ‘Next >’ button. The following window will then be displayed. Simply click ‘Next >’.



The following window will then be displayed. Again, click ‘Next >’.



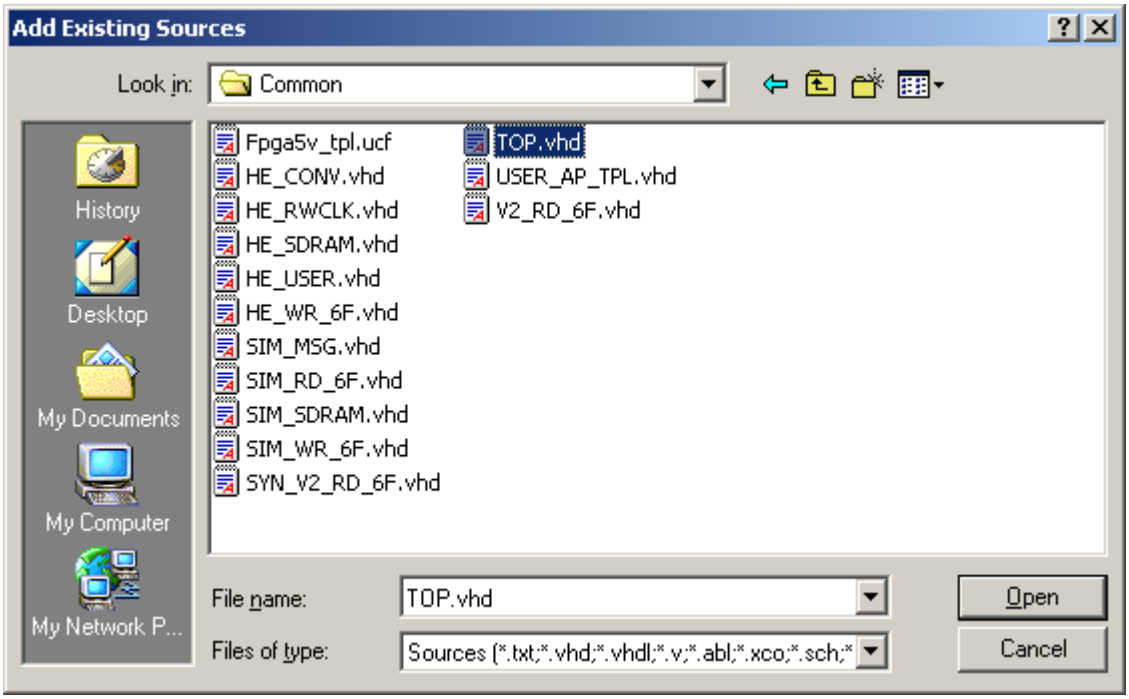
Finally, the following window is displayed providing a summary of all the project information you have entered. Click ‘Finish’ to make the new project file.



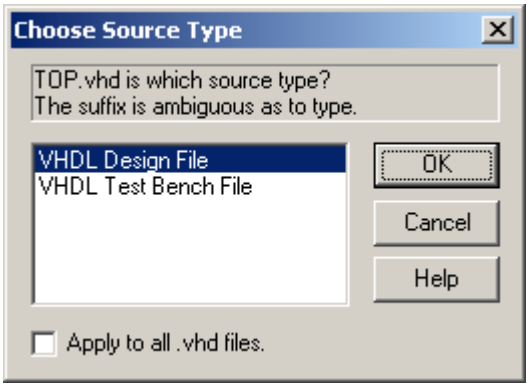
Step 3: Adding VHDL Source to the New Project

The next step is to add design source, starting with the top level of the hierarchy. For all FPGA module projects the top level of the design is always contained in the file 'top.vhd'. 'top.vhd' is always provided as part of the 'Common' directory for each module type.

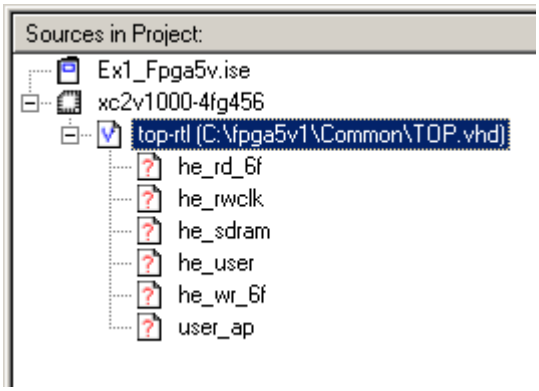
Select the menu item 'Project→Add Source…'. The following window will be displayed where you will need to navigate to the 'Common' directory that was created on your local drive. Select the file 'top.vhd' and click 'Open'.



The following window will then appear. Select 'VHDL Design File' and click OK to add 'top.vhd' to the project.

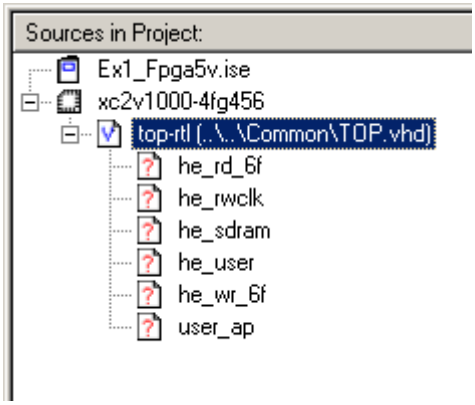


With this done, the Module View window may look something like the picture below.



In this picture we can see that the path shown for 'top.vhd' is absolute. That is, it shows the complete path. The project needs to be changed to use relative path information. To do this, left click on the entity 'top'. With top selected, right click to bring up a menu and select 'Toggle Paths'.

The Module View should now look similar to the picture below, depending on the particular source files that are required by the module type you are using. Note, the path information has now changed to reflect a relative path to the Common directory.



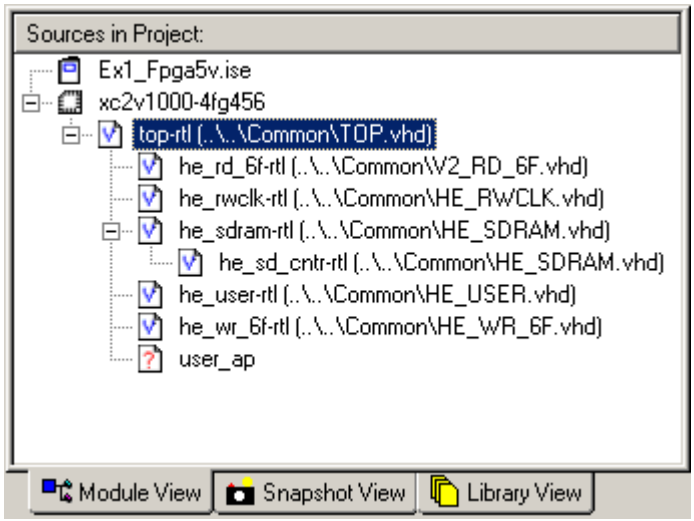
In the case of the FPGA5v1 example conversion, after adding 'top.vhd' we can now see 6 more design entities are needed. One of these entities is the User-Application level of the design which contains the VHDL that makes this example the getting started example, Example1. The other entities shown are part of the Hardware Interface Layer and are found in the 'Common' directory.

First add the appropriate files from the 'Common' directory in order to replace the red question mark icons with correct entities. To do this, you will again need to use the 'Add Source…' menu item. Navigate to the 'Common' directory and select the files that have names that match the entities in the Module View of your new project.

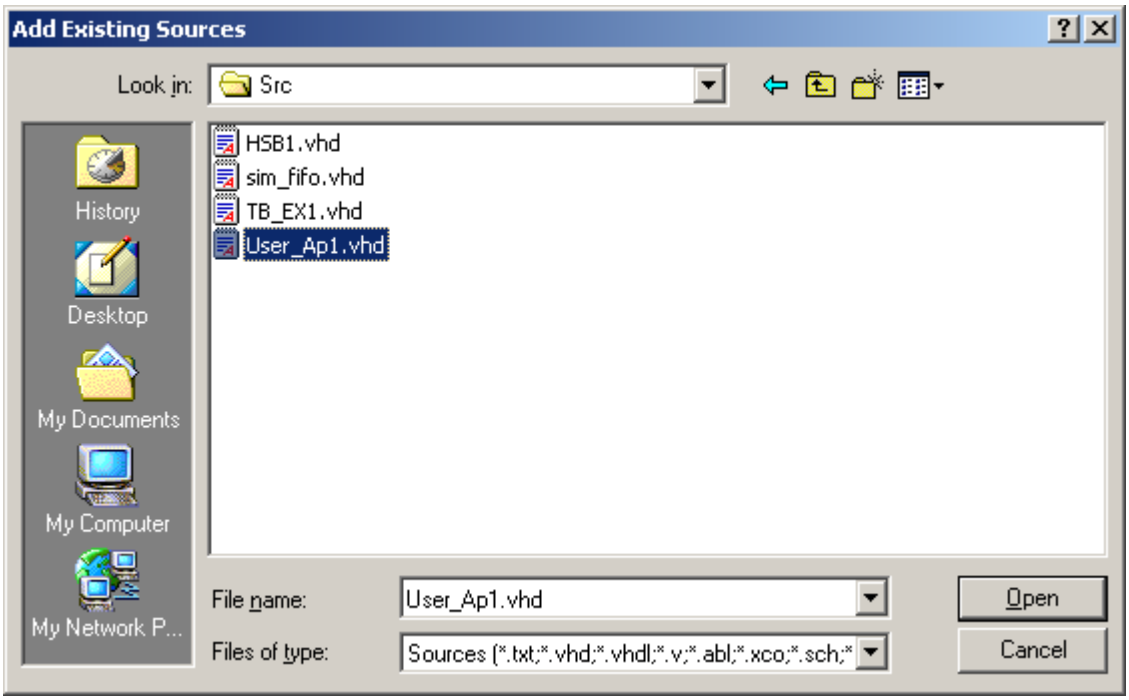
Please note: the HE_RD_6F entity is provided in the 'Common' directory in the source file 'V2_RD_6F'.

When adding each file, the correct Source Type will be 'VHDL Design File' as was selected when adding 'top.vhd'.

When you have added all required Hardware Interface Layer components the Module View should look similar to the picture below for the FPGA5v1 conversion:



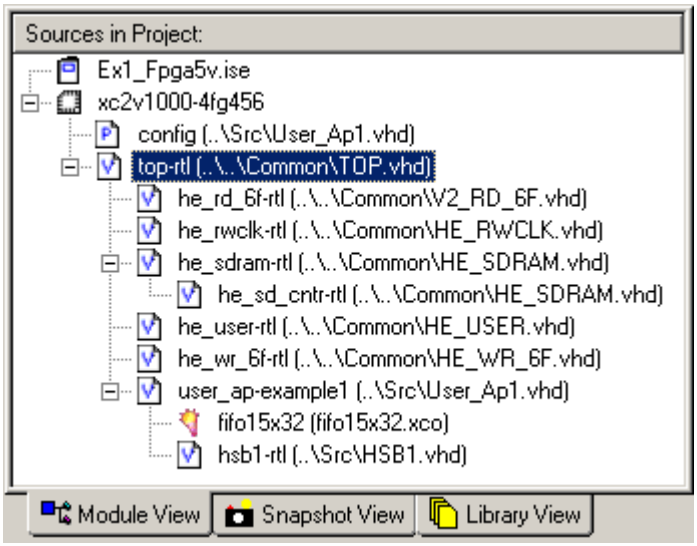
Next you will need to navigate to the 'Src' directory of Example1 and add the User_Ap file to the project:



After the 'user_ap' entity has been added to the project you will see which other source files are required below this entity. Add the appropriate source files from the 'Src' directory.

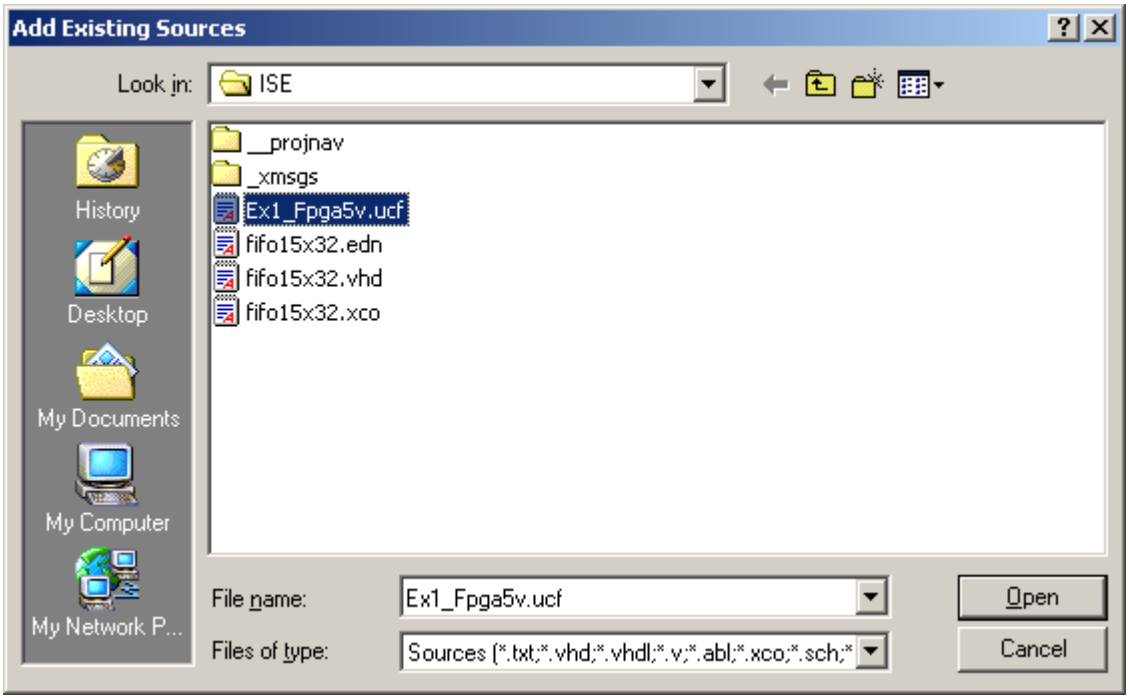
After you have added all of required VHDL source files from the 'Src' directory there may still be red question marks against entities in the hierarchy. These entities will correspond to Core Gen components that are placed in the Example1 'ISE' directory. In the case of Example1 there is one Core Gen component called 'fifo15x32' that must be added to the project from the 'ISE' directory.

With all relevant VHDL source added to the project the Module View should look similar to the picture shown below for the FPGA5v1 conversion:



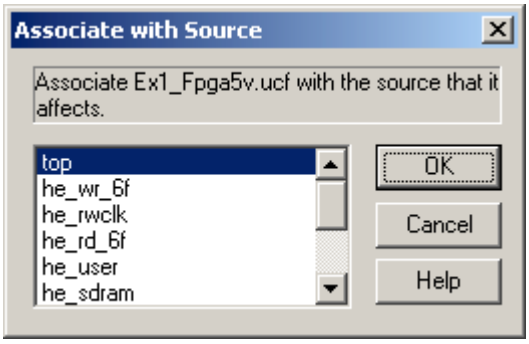
Step 4: Adding User Constraints

The next step is to add user design constraints to the project. Using 'Project→Add Source…' add the user constraints file contained in the 'ISE' directory of the project.



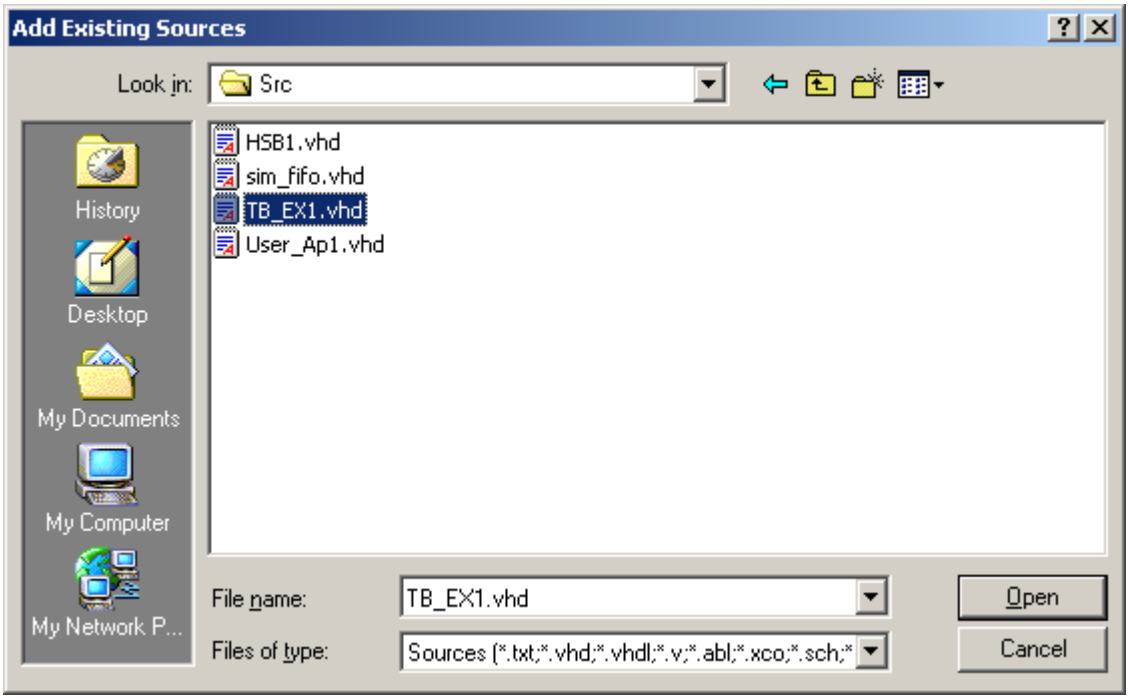
Select the UCF file and click 'Open'.

The following window will appear to allow you to specify the design file to which the user constraints should be associated. Highlight 'top' and click 'OK'.

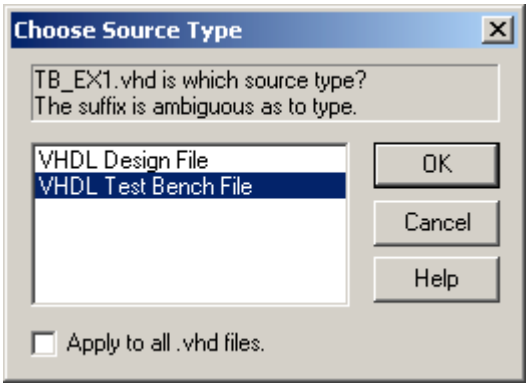


Step 5: Adding a Simulation Test-Bench

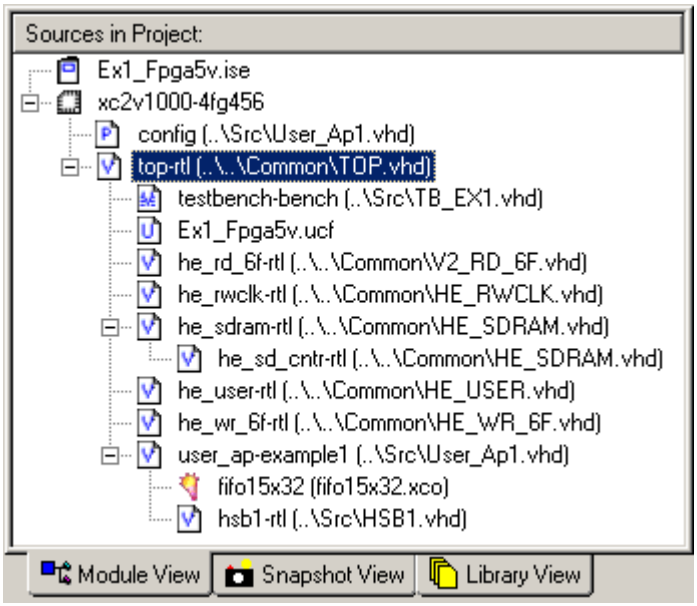
Typically, a project will also include a test-bench for simulation. For Example1 there is a test-bench provided in the 'Src' directory of the project. This file must also be added to the project using 'Project→Add Source…'. Navigate to the 'Src' directory, highlight the file that beings 'TB_' and click 'Open'.



The following window will appear where you need to specify the source type. Select 'VHDL Test Bench File' and click 'OK'.



At this point the Module View should look similar to the picture shown below for the FPGA5v1 conversion process.

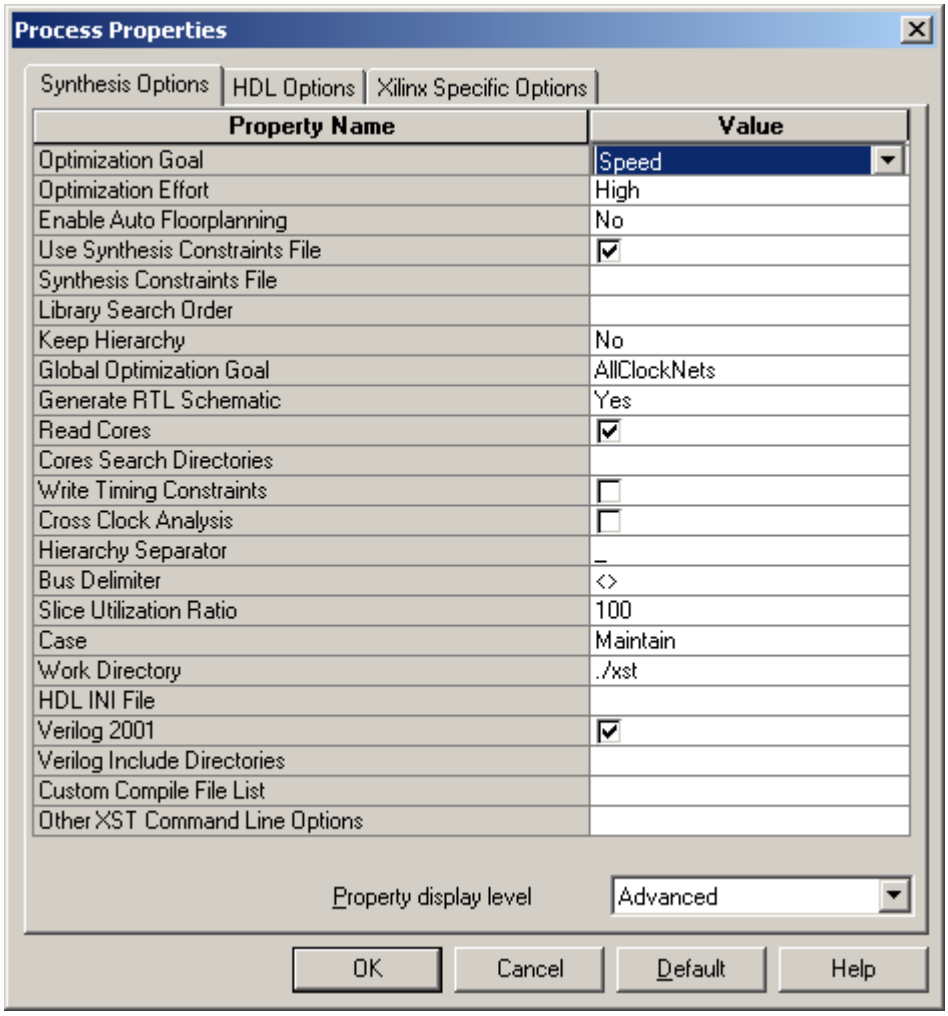


Step 6: Setting Project Build Options

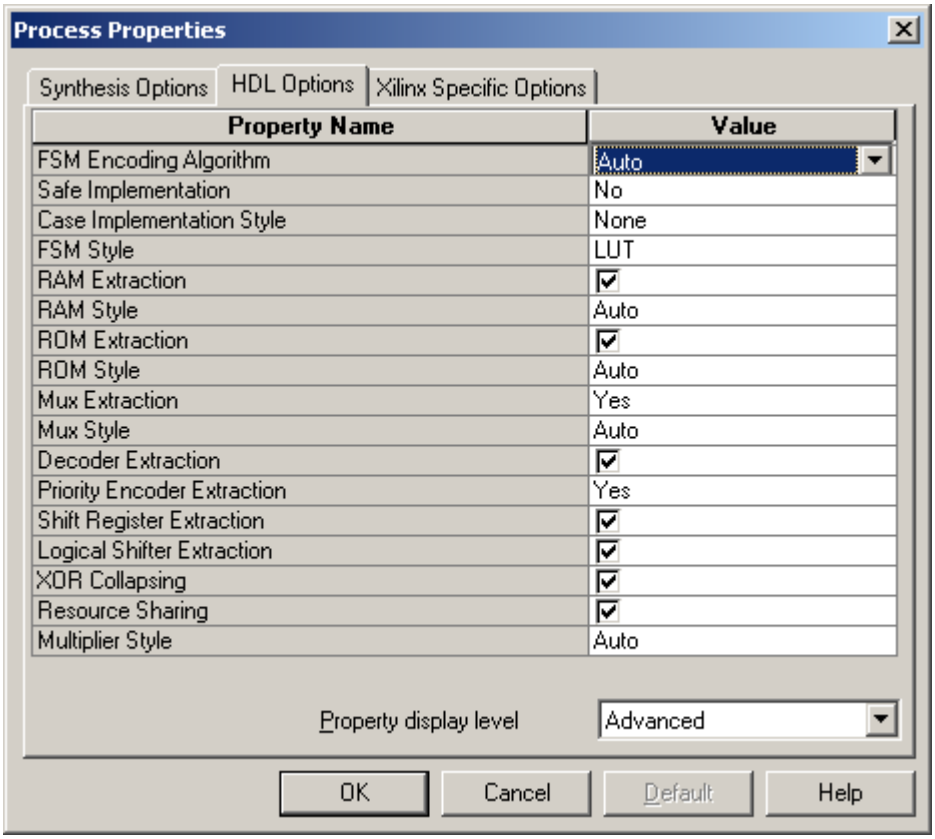
The last step in creating a new project is to apply the necessary project settings that will allow the design to be built correctly.

Ensure the file 'top.vhd' is highlighted in the Module View, and then right click on 'Synthesize' in the Process View. Select 'Properties…' to open the following window.

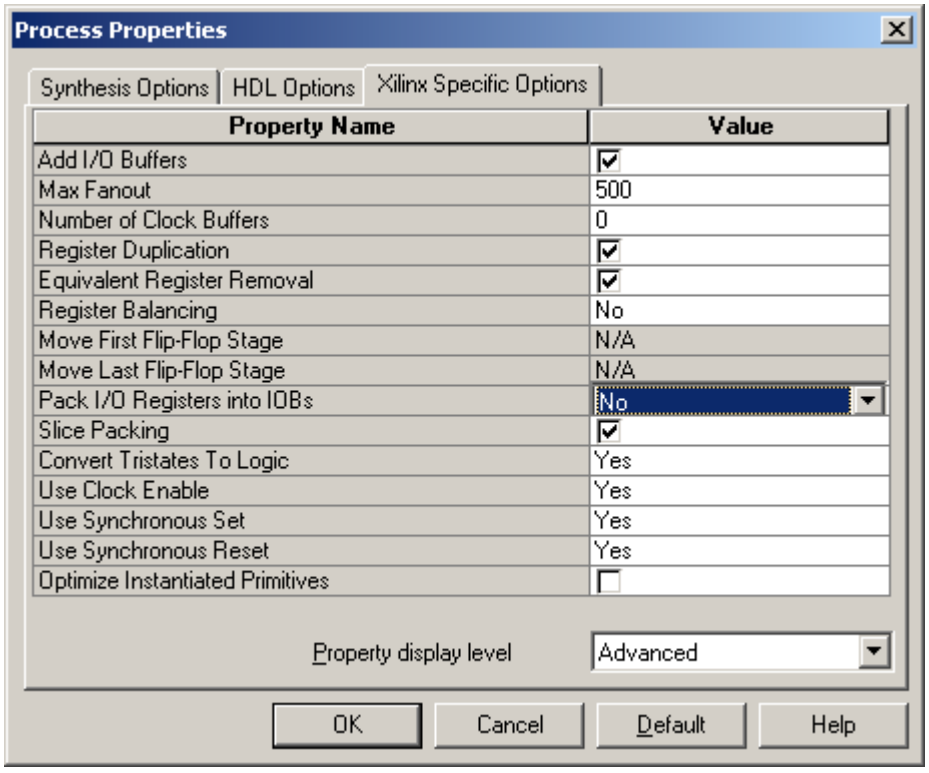
With the 'Synthesis Options' tab at the front, set 'Optimization Effort' to High and set 'Hierarchy Separator' to '_'. Having done this check that the settings match those shown below.



Next bring the ‘HDL Options’ tab to the front and check that the settings match those in the picture below.

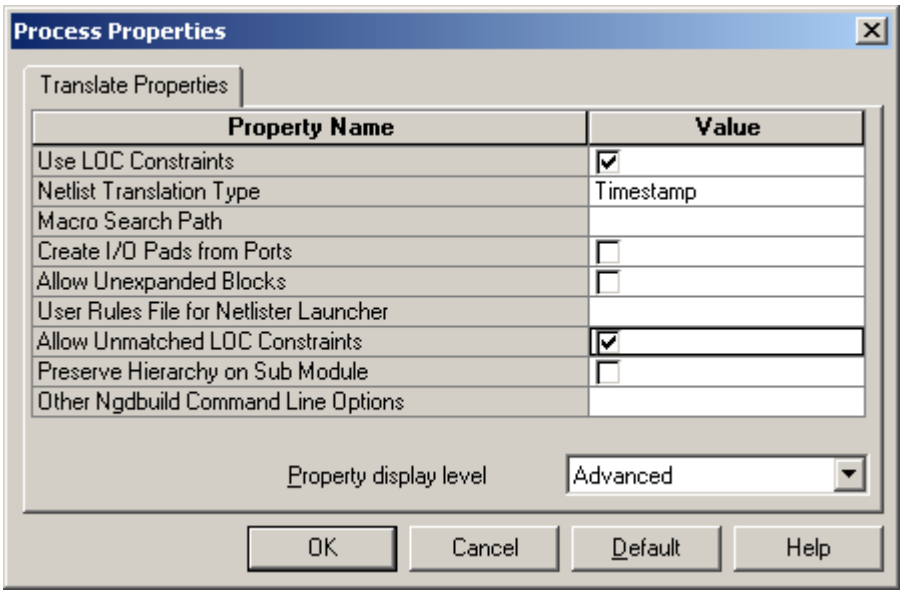


Next bring the ‘Xilinx Specific Options’ tab to the front. Change the ‘Number of Clock Buffers’ item to ‘0’, and set the ‘Pack I/O Registers into IOBs’ item to ‘No’. With this done, check that the settings match those in the picture below.

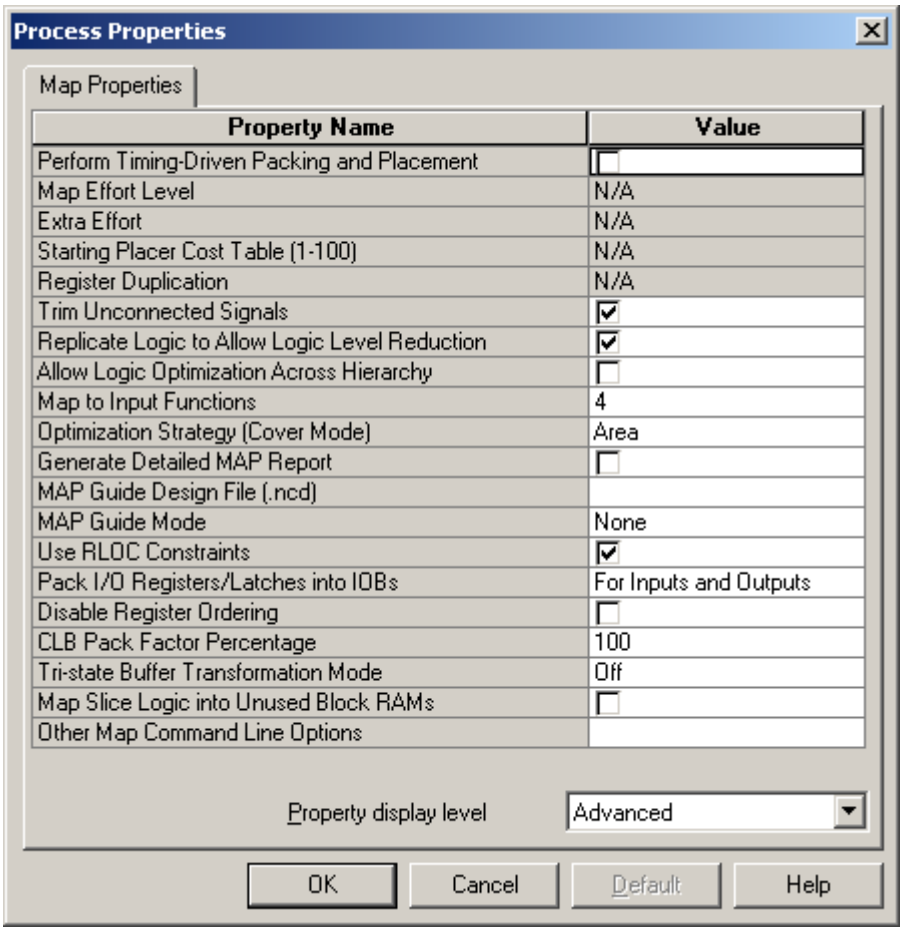


Click on the ‘OK’ button at the bottom of the window to apply the new settings.

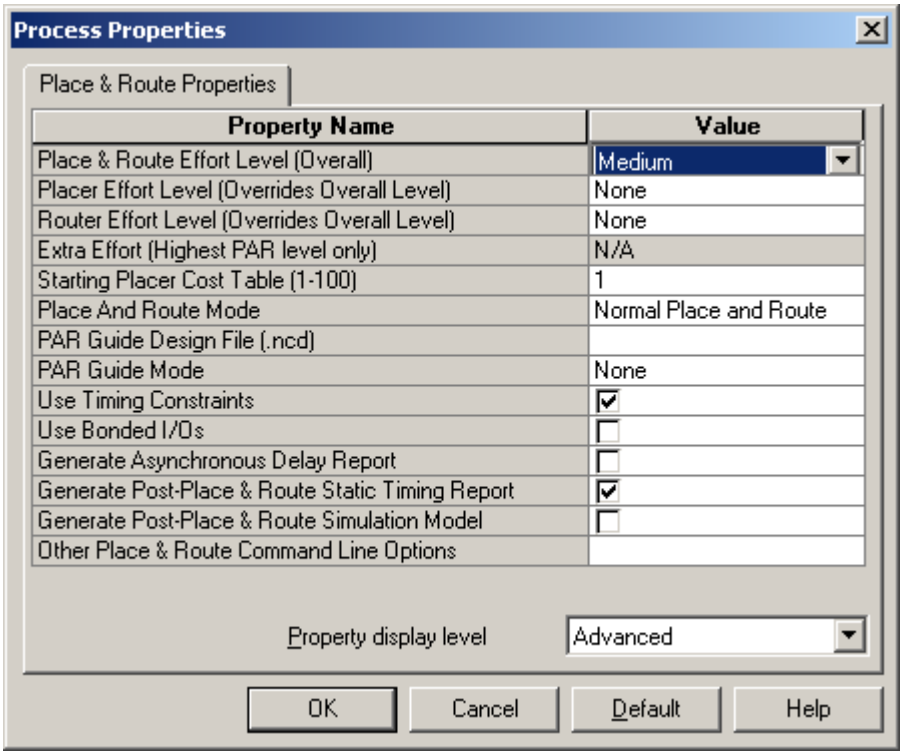
Next the Translate Properties must be checked. With the file ‘top.vhd’ still highlighted in the Module View right click on ‘Translate’ in the Process View. Select ‘Properties…’ to open the following window. Tick the item ‘Allow Unmatched LOC Constraints’, check all other settings match, and click ‘OK’.



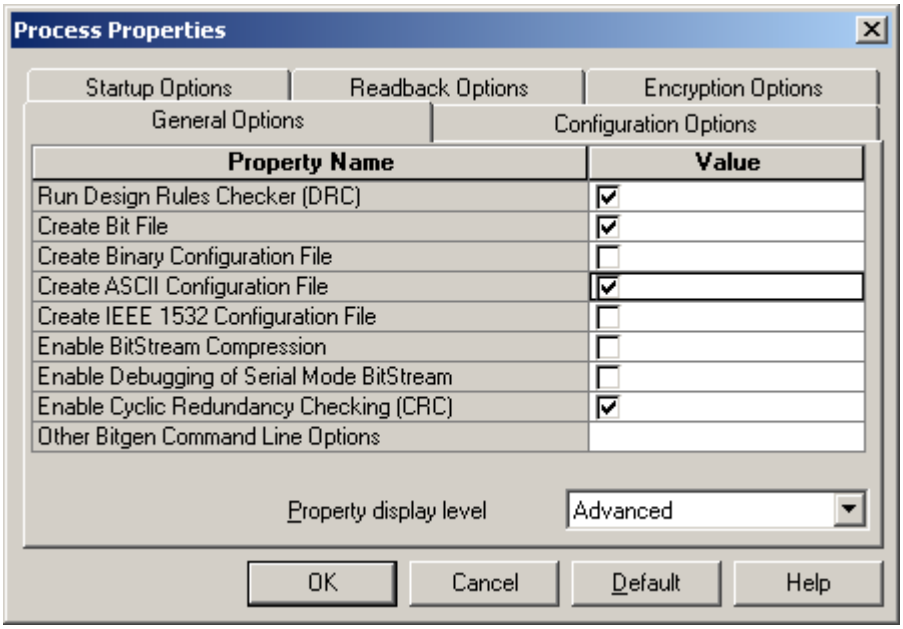
Next open the Process Properties window for the Map process. Check that the settings match those in the picture below.



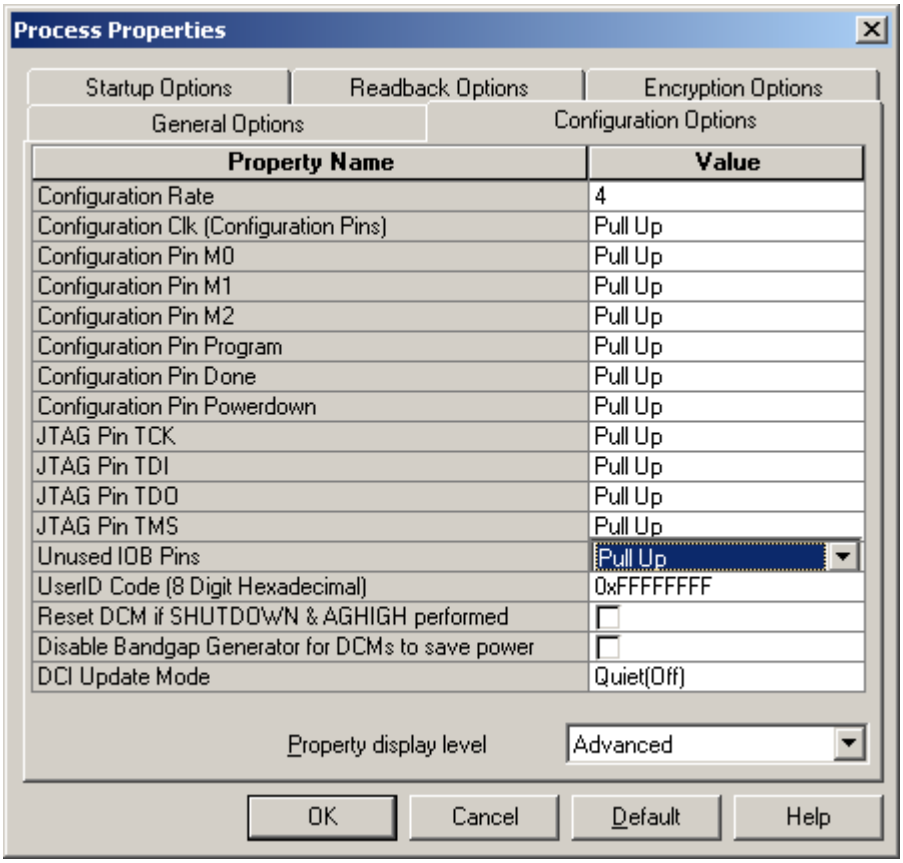
Next check the Place and Route process properties. For Example1 the 'Place & Route Effort Level (Overall)' typically needs to be set to 'Medium'. Make this change and check all other settings match the picture below and click 'OK'.



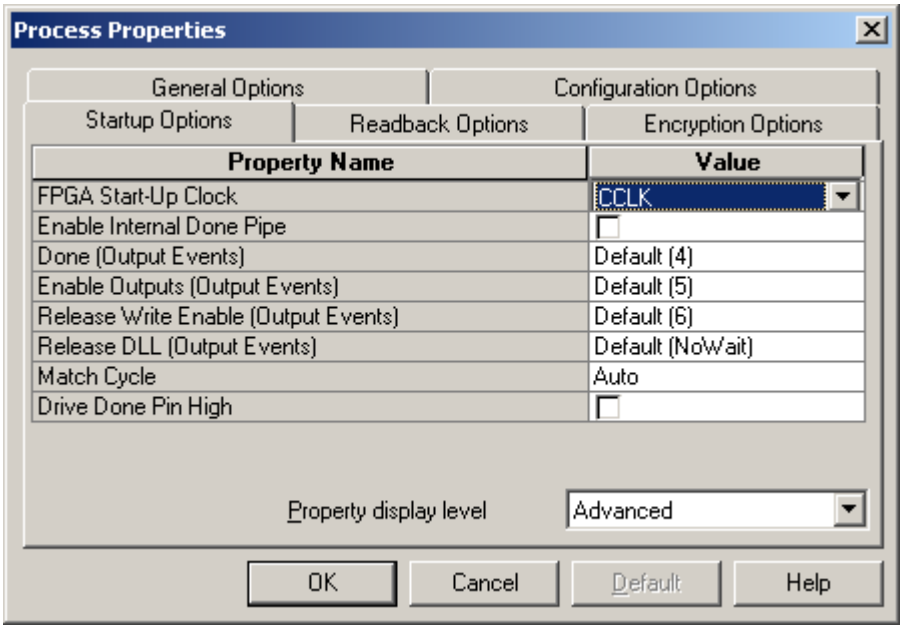
Next check the 'Generate Programming File' properties. With the 'General Options' tab at the front, tick the 'Create ASCII Configuration File' and then check that all other settings match for this tab.



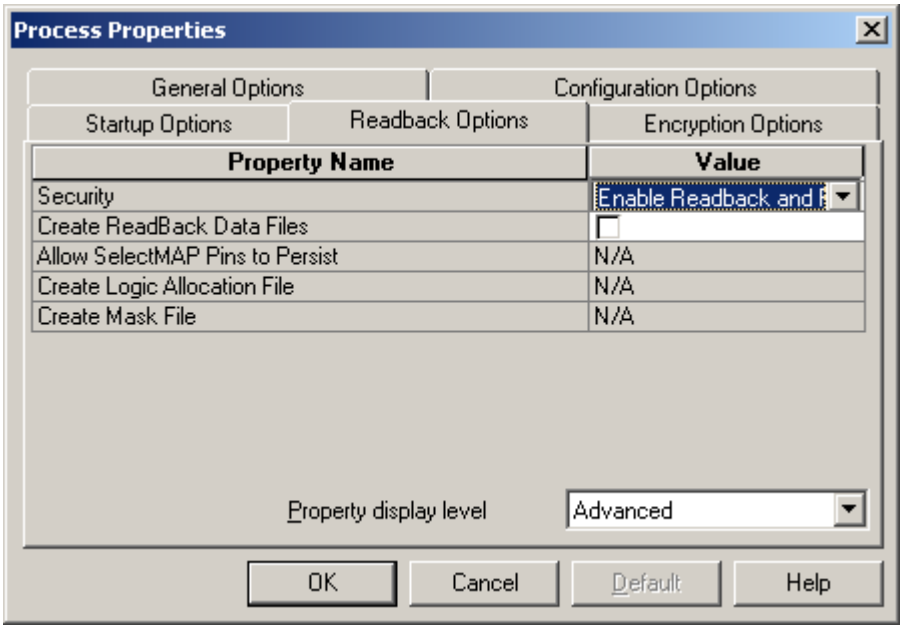
Bring the Configuration Options to the front. Select 'Pull Up' for the 'Unused IOB Pins' item. With this done check the settings match those shown in the picture below.



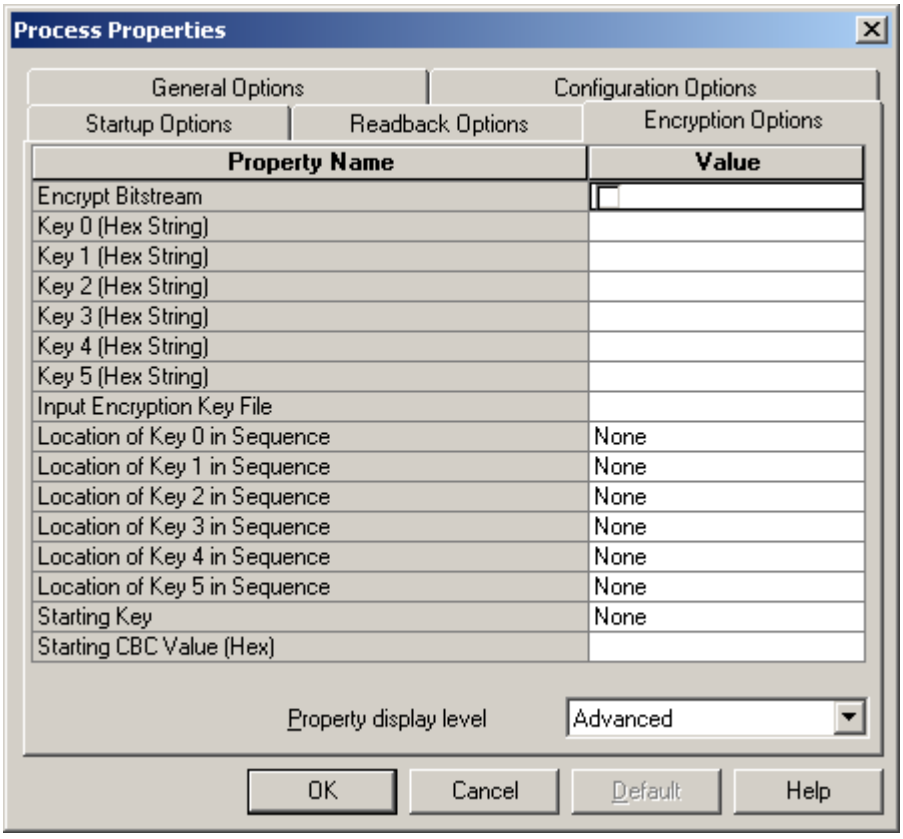
Next check the settings for the 'Startup Options' tab against those shown in the picture below.



Next check the ‘Readback Options’ against the picture below.



Finally check the ‘Encryption Options’ tab against the picture shown below.



When all tabs have been checked, click ‘OK’ to enter the new settings.

Step 7: Building the Project

At this point the project is ready to be built. All of the required design files have been added to the project and the project build settings have been checked. Example1 should now build as far as bitstream generation without error.

Although each example project supplied on the HUNT ENGINEERING CD will differ from Example1, the process to create a new project for ISE 7 is the same. The routine described in this section can therefore be repeated for each of the standard examples provided on the CD.