HUNT ENGINEERING
**Chestnut Court, Burton Row,
Brent Knoll, Somerset, TA9 4BP, UK
Tel: (+44) (0)1278 760188,
Fax: (+44) (0)1278 760199,
Email: sales@hunteng. co.uk
http://www.hunteng.co.uk
http://www.hunt-dsp.com**

HERON

Hunt Engineering ResOurce Node

Specification

Document Rev B

P.Warnes 22/08/02

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Document revision	Changes
Preliminary	First written
1.0	1. Re-allocated the pins used to multiplex additional address lines onto, for use in a “special” slot. Rename Addr/Blocksel pin to Addr/Flagsel. Note this change was made after HERON1 was designed so this module does not comply to this part of the HERON specification. 2. Define the C6000 module optional connector positions 3. Correct the timings for the 167Mhz FIFO accesses 4. Correct the peripheral interface timings. 5. Add explanation of the use of the peripheral interface. 6. Add explanation of the intended use of the different FIFO flags.
A	1. Add 100Mhz “HEART” compatible timings 2. Add reference to separate HSB spec 3. Correct some pin names 4. Defined Signal Voltage levels 5. Clarify the dimensional drawings of the connector
B	1. Corrected the setup time for WE in 100Mhz FIFO timings

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Purpose

Having been successful in developing modular solutions for Real Time DSP, over a period of some ten years, HUNT ENGINEERING wanted to have a module standard suitable for use with today's high specification DSPs like those in the C6000 family from Texas Instruments (TI) or the Virtex family of FPGAs from Xilinx.

We are able to learn from other module standards like the TRAM standard from Inmos and the TIM-40 specification, (which we had some influence over), published by TI. We need to take on board the advantages of these past standards, and to consider the problems we have encountered in using those standards over our ten-year history.

The first point is that both of the module specifications named above were processor specific. This gives problems in two areas; the module is specified to always have a processor (making it difficult to have modules without one) and it was not possible to update the processor type used in a system without switching to a completely new board set.

What we aim to do with HERON modules is to provide a module format that can truly provide nodes in a nodal system, i.e. there is no advantage or disadvantage to having a processor on a particular module. We also want to provide a module that can grow with our requirements into the future. This is both in terms of choosing different processor types, and in terms of allowing greater performance as silicon chip technology moves on (as it inexorably does).

To achieve this we will use a FIFO interface. There will be a FIFO (or FIFO like) component on the module carrier board directly connected to the module sockets. The module will simply access that synchronous FIFO interface by supplying a FIFO clock of its own choosing, and then using read and write enables and flags to determine when data can be received or sent.

In fact HUNT ENGINEERING have had such an interface before, used for the GDIO modules. The HERON specification is an enhancement of that GDIO specification, and the legacy GDIO modules can be used in a HERON socket, with some restrictions on functionality.

Another thing that we have learnt from the previous module specifications is that a modular system must pay attention to mechanical stability if it is to remain reliable throughout its life. The HERON module therefore has four fixing holes per module, and uses a very robust connector.

Capabilities

The HERON module is capable of transferring data in both directions simultaneously, in either a 32- bit word width, or operating in a legacy 16 bit mode. The module itself will control the speed of the transfer, as it provides the clocks for the synchronous FIFOs. The limit in speed, however, is the commercial availability of FIFO like devices (perhaps FPGA implementations of FIFOs in some cases. Initial designs are based on the availability of 67 to 100 Mhz parts, allowing 264 and 400 Mbytes/second simultaneously in and out!

Is it a standard?

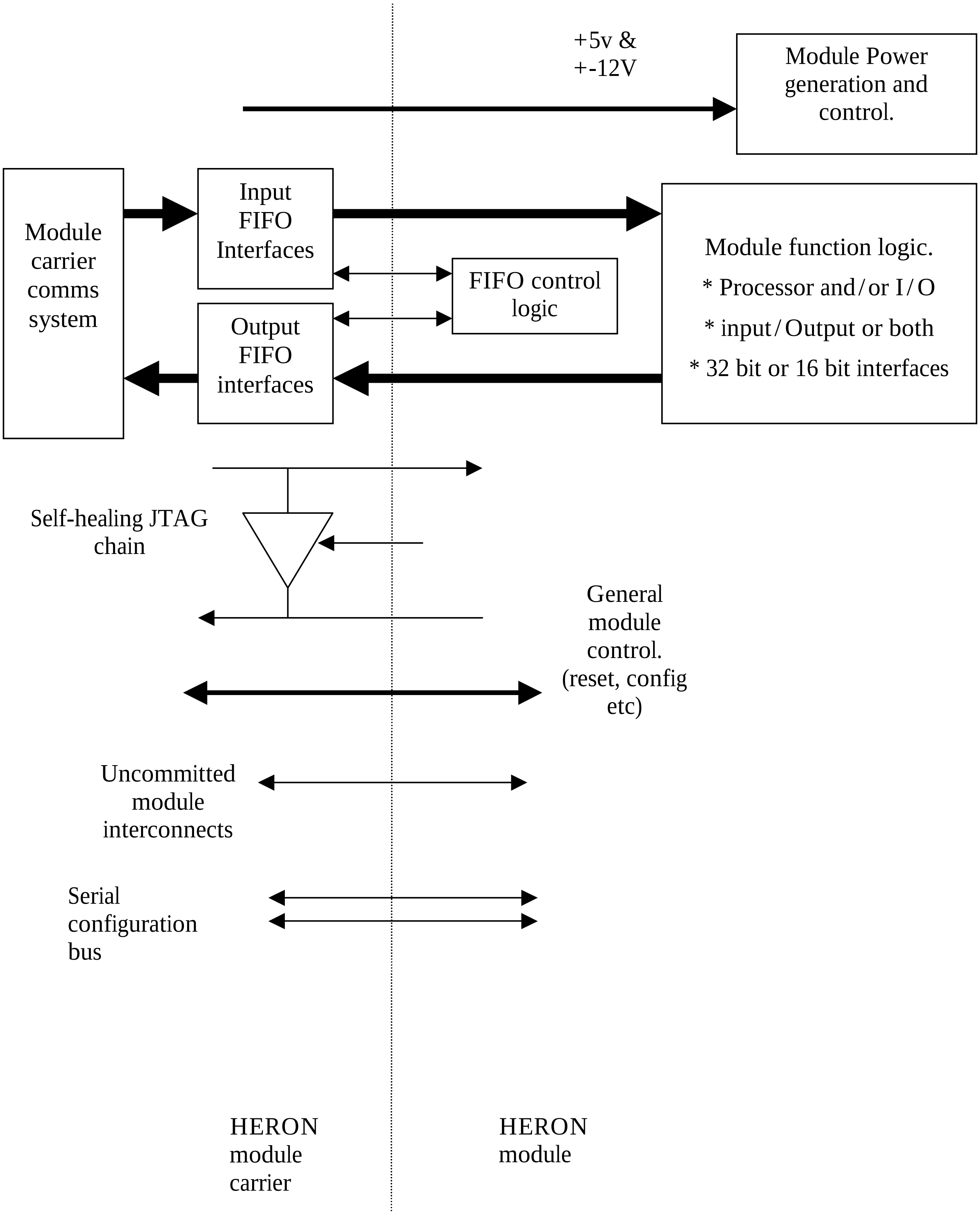
Well that depends on your definition of a standard. It is published freely in this document available from a number of sources. For example the latest version will always be available from www.hunteng.co.uk.

It is not and will not, however, be registered or adopted by a standards-raising body.

The interface to the module carrier is fully defined in this document, allowing modules or carriers to be designed by parties other than HUNT ENGINEERING. While HUNT ENGINEERING will not offer any validation of second or third party designs we will as always endeavour to support our customers fully in what they are trying to do. All we ask is that you discuss what you are trying to do with us at the outset so that we have the chance to make suggestions and recommendations.

Our business is based around supporting the future of our customers, and making it easy to progress from one stage of a project to the next. This means that it is a primary goal of ours to continue to use the same module specification unchanged. It may be necessary however to enhance or extend this specification to cater for eventualities that we have not foreseen. In this case we will strive to maintain backward compatibility so that older HERON products will always be useable in our systems. This however is not a commitment to do so, and HUNT ENGINEERING cannot accept any liability for problems caused by changes made to this specification.

Schematic of the HERON module interface



FIFOS

The main interfaces on the HERON module are the FIFO interfaces. This specification allows for six FIFOs in each block, that is, six input and six more for output. In this specification input FIFO will always refer to those used for providing data to the module. Following that all references to output FIFO will refer to those used to accept data from the module.

It is important to remember at all times that the actual FIFO component is fitted to the module carrier board, NOT the module.

JTAG (IEEE 1149.1 test bus)

There is a JTAG chain allowed for on the module carriers that will pass the JTAG serial TDI/TDO chain through each module on the carrier. If there is no module fitted to the module site, or a module is fitted that does not assert the presence detect signal, the module carrier will ensure that the TDI/TDO connection is made for that module site. This JTAG chain is controlled by the module carrier using a TI 8990 Test Bus Controller. As such it will be used for running debug tools like those available for TI DSPs. It might not be useful for “other” JTAG connections however (like the Xilinx PROM programming, or device debugging) as their controlling software may not be compatible with the 8990 hardware. In that case additional JTAG connections will be made to the modules using connectors that are not defined as part of this spec.

Power Supply

While it is recognised that technology today is demanding lower and lower supply voltages like 3.3v and 2.5v, it has been decided that HERON modules should provide these supplies themselves as and when required. The HERON module provides the +5v and +-12V available to almost all of the standard Card formats in use today (ISA/PCI/VME/cPCI etc)

This means that I/O modules can generate their own regulated and smoothed power planes if required by the logic. Analogue I/O for example would follow this example. Processor modules can generate whatever voltages the processor and associated logic requires. This allows for the use of future technology without needing to change the HERON module specification, or Carrier board design.

General module control

There are some general control signals like reset and config. They are each described separately in a later section of this document. There is also a HERON Serial Bus (HSB), that allows any module to address any other module. This can then be used to transfer non real time configuration type information.

Uncommitted Module interconnect

Sometimes direct connections are desirable between modules, e.g. for using processor timer pins to clock I/O modules, using I/O modules to interrupt processors etc.

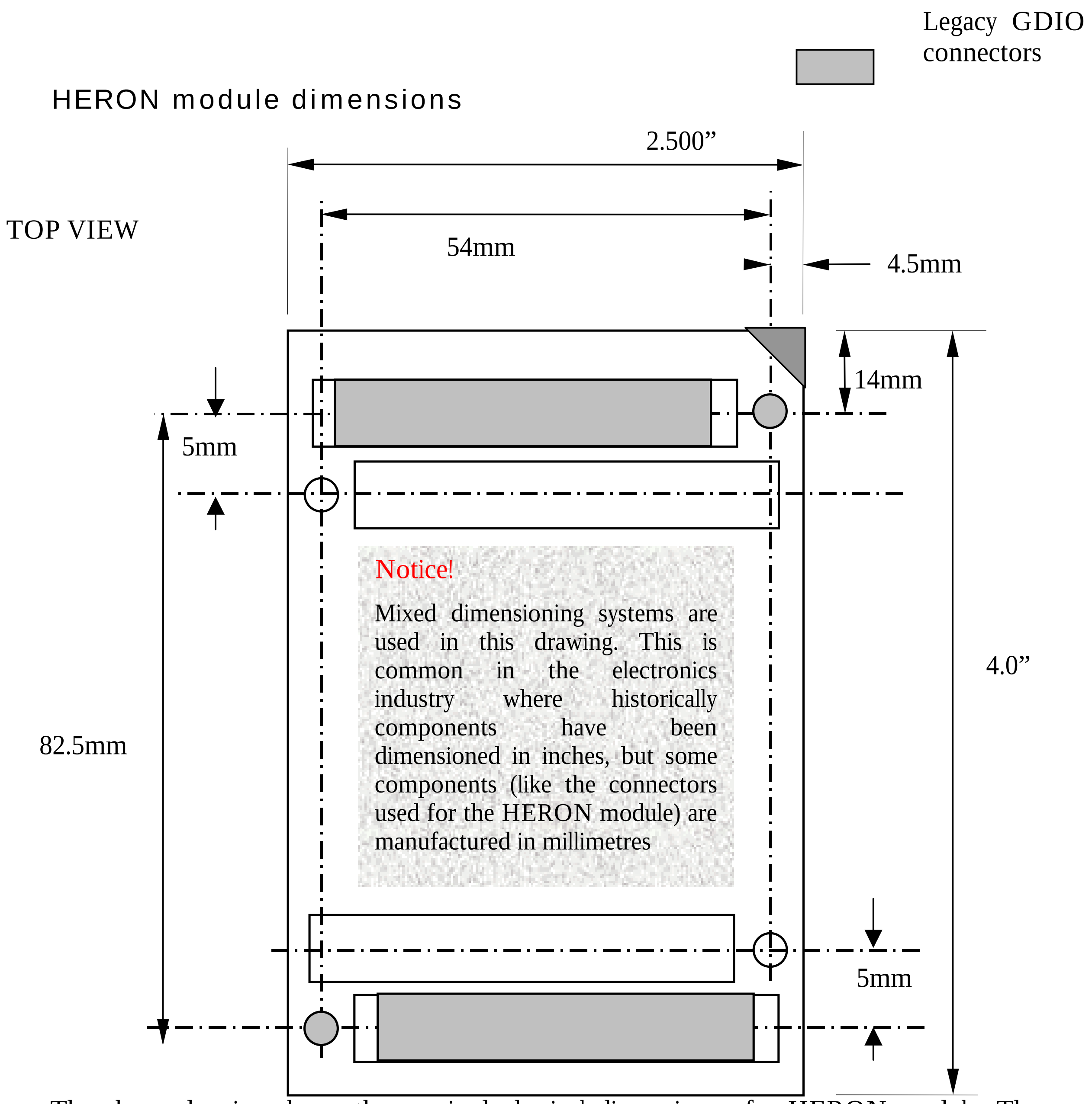
Therefore the HERON spec allocates some pins that are simply connected together on all module sites of that carrier. They are not buffered or committed to a particular function, but are simply there for certain application modules to use as they see fit.

The HERON connectors are chosen to be a superset of the 2nd generation GDIO module connectors, which we describe as “Synchronous GDIO”. These connectors are quite high-density while retaining robustness.

The Module carrier provides four 54pin sockets, which are 2mm pitch connectors like part numbers SMM-127-01-S-D from Samtec Inc. The legacy 50 way GDIO connectors will also fit these larger connectors.

The HERON Module uses four 54 pin headers which are 2mm pitch, like part numbers TMM-127-03-G-D from Samtec Inc.

When mated these parts give a board to board spacing of 6mm.

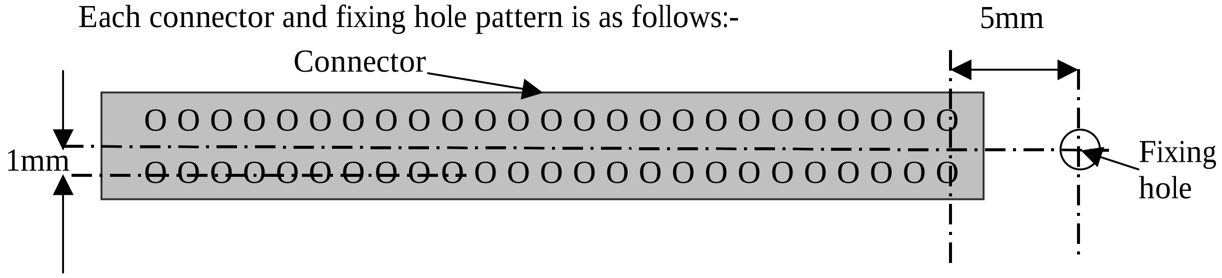


Notice!

Mixed dimensioning systems are used in this drawing. This is common in the electronics industry where historically components have been dimensioned in inches, but some components (like the connectors used for the HERON module) are manufactured in millimetres

The above drawing shows the required physical dimensions of a HERON module. The drawing shows the position of four fixing holes, and four 54-way connectors.

Each connector and fixing hole pattern is as follows:-

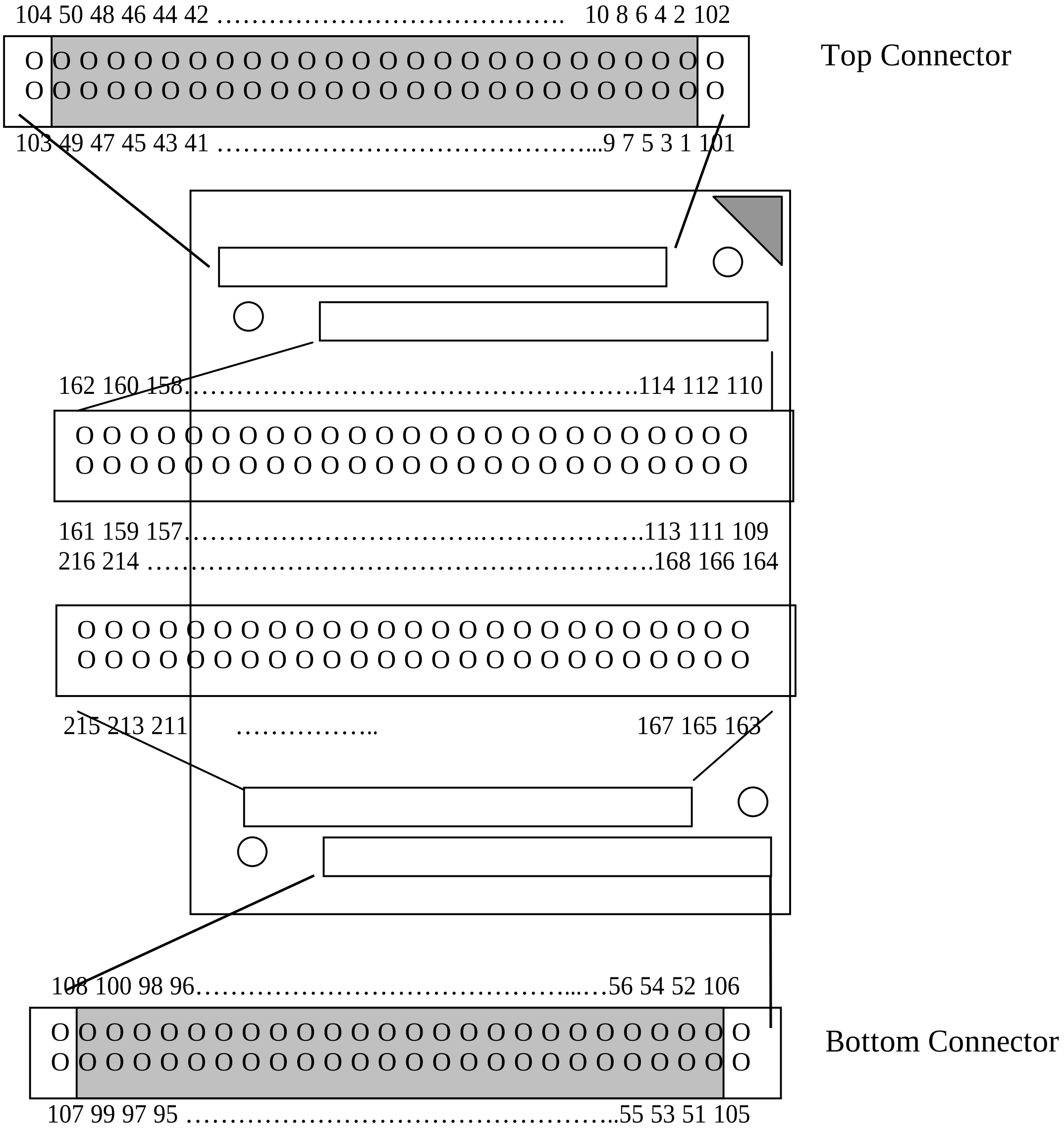


The fixing holes have a diameter of 0.125" providing a clearance hole for an M3 fixing, and the connectors use a hole diameter of 0.030”, which is large enough to accept the pins.

The dashed lines —·— show the centres of the holes. The connector holes have a pitch of 2mm on both axes, so the connector centre line is 1mm from the centre line of each row of holes. The fixing hole is aligned with the centre line of the connector.

HERON Connector Pin numbering

The diagram below shows the pin numbering used for the four 2x27 pin connectors. Please note that the Connectors used by the legacy GDIO were already numbered 1-100. The extra pins on these connectors are numbered 101-108, and the two extra connectors use the pins numbered 109-216.

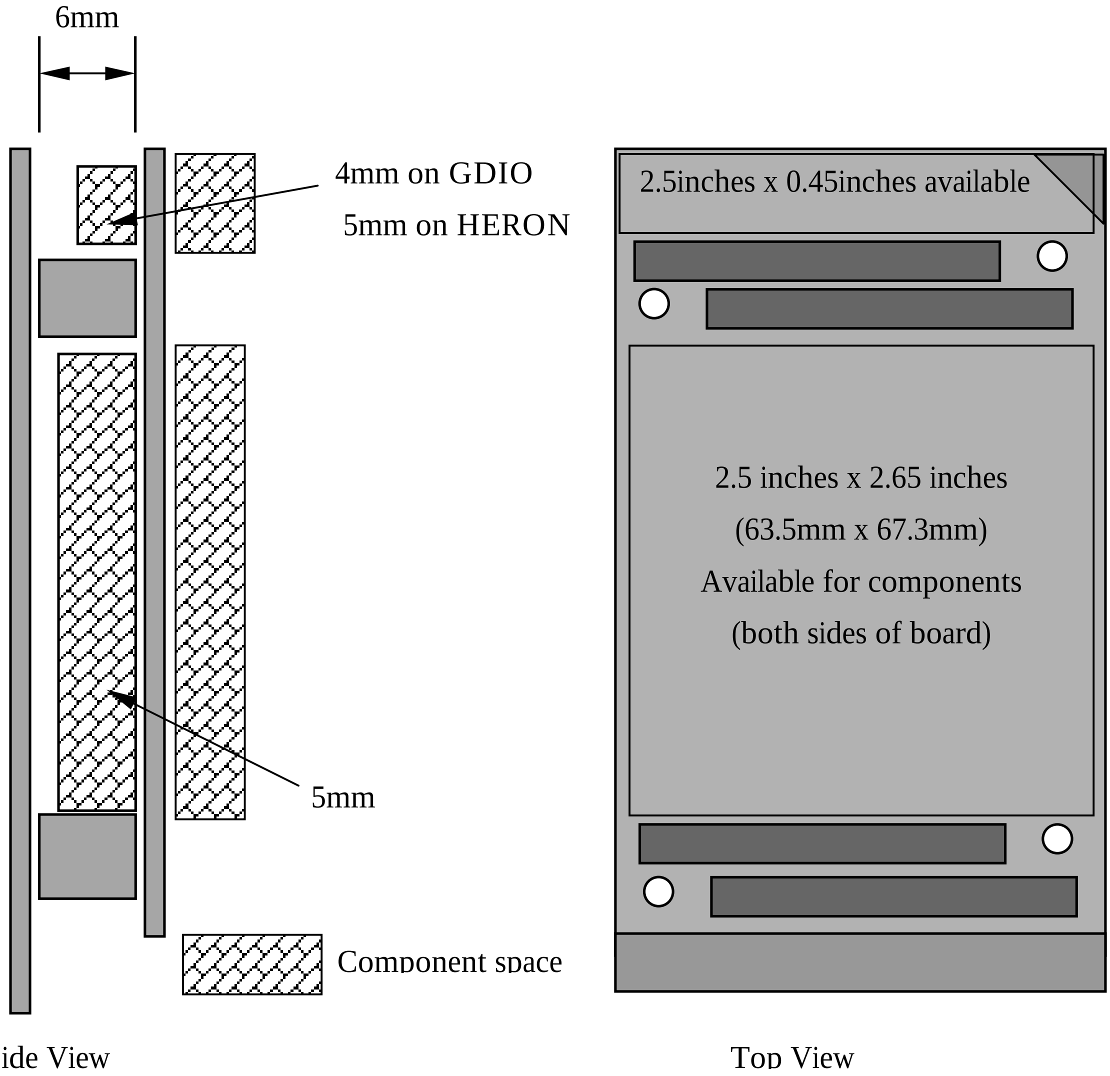


Available component areas

When using the recommended connectors on the HERON module, the assembly results in a spacing of 6mm between the top of the base board PCB, and the bottom of the HERON module PCB.

The Module Carrier boards should have no components fitted under the HERON module sites, but if necessary through hole components can be fitted from the reverse of the board, and soldered on the module side of the carrier card. If this is done, the leads must be cropped so that the total height of the component lead and solder joint does not exceed 1mm.

For this reason, and to allow some flow of cooling air, any components placed on the underside of the module must remain below a certain height. The diagram below indicates the available space for component spacing. Note that in the area where the module protrudes past the (1-50) connector there is an anomaly between GDIO and HERON spec boards. This is because the GDIO series could be fitted to an HETBASEIO, and there was the TIM connector fitted in this area. This anomaly however is not a problem as HERON carriers can still accept boards designed within the GDIO limit, and HERON modules can never be fitted to GDIO only carriers like the HETBASEIO.

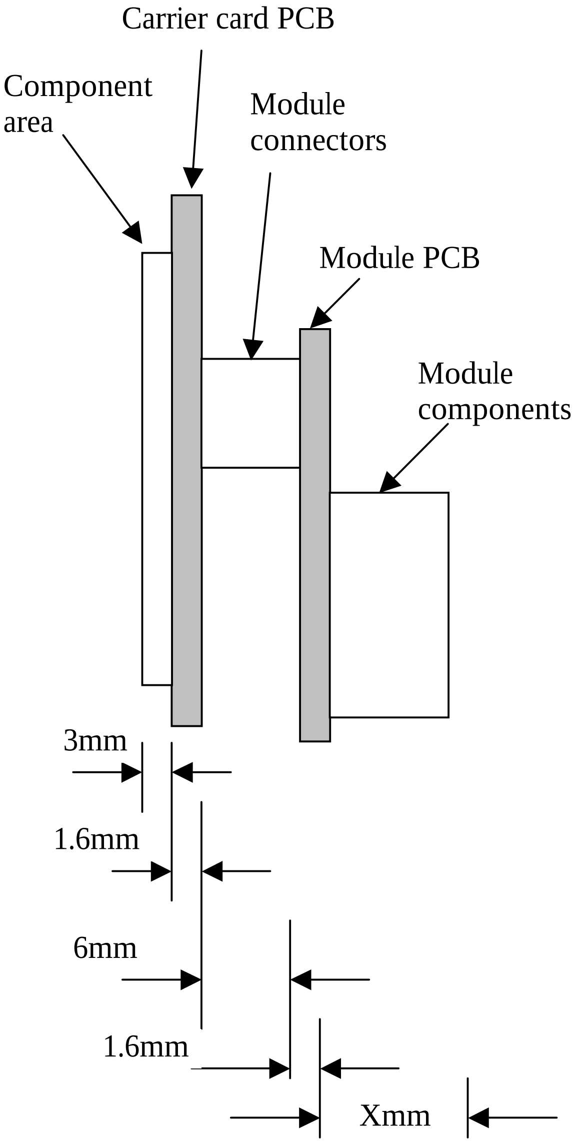


Recommended uses of areas

The GDIO module, and hence HERON module has an overhang above the top connectors. This is intended for regulators, or switch mode circuits that are needed to provide Analogue power supplies, or lower voltages for low voltage logic. For this reason the power supplies to the module are situated on the first (topmost) connector, near to this area.

If no power control logic is required however, this area can be used for any components including connectors for I/O signals.

The Component space on the upper side of the module (the one furthest from the carrier card) has no restriction on height. However, the overall assembly thickness of a carrier card and a module is calculated as below:-



In PCI, ISA, VME and cPCI systems the normal slot spacing is a little more than 20mm, making a sensible single slot card be 20mm. So, in order to allow a single slot assembly a HERON module would require X to be less than 7.8mm.

It is recognised, though, that an I/O module must have I/O connectors, and it is unlikely that these connectors, along with their associated cable connectors, could result in an assembly where X is less than 7.8mm. In this case a carrier fitted with the module would require an empty slot adjacent to it.

Modules with subsets of the connectors

In order to maintain backwards compatibility with the GDIO modules, it is possible to fit 16 bit I/O modules to a HERON module slot. It is also envisaged that there could be new modules designed that will not need all of the features of a full HERON module implementation. In this case a 16 bit I/O module can be used (having only two connectors fitted), or even a 32 bit I/O module with three out of four connectors used.

The connector pin outs have been carefully selected to allow this.

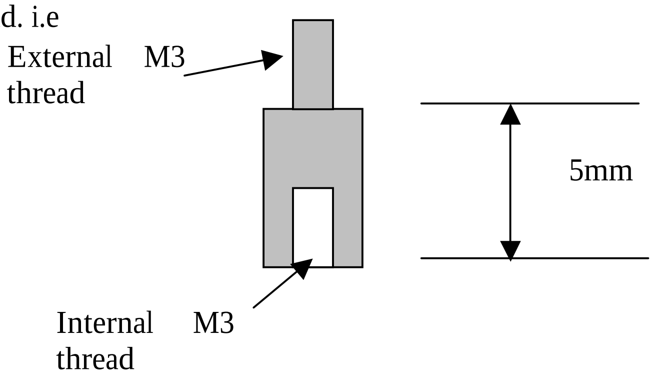
In any case, if a module is manufactured with one or more of the HERON connectors not present, there is a height limit of components on the underside of the board, in the area where the carrier board would have its connector.

The height limit is 2mm.

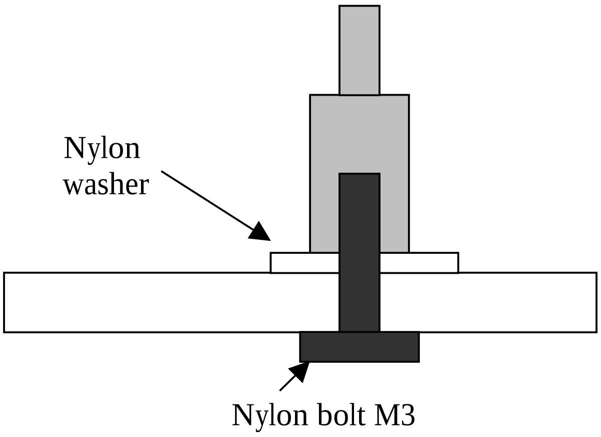
For carrier cards that need only accept GDIO modules, refer only to signals on pins 1 through 100. All other signals can be ignored as they are not present on a GDIO format module.

Mechanical retention of modules

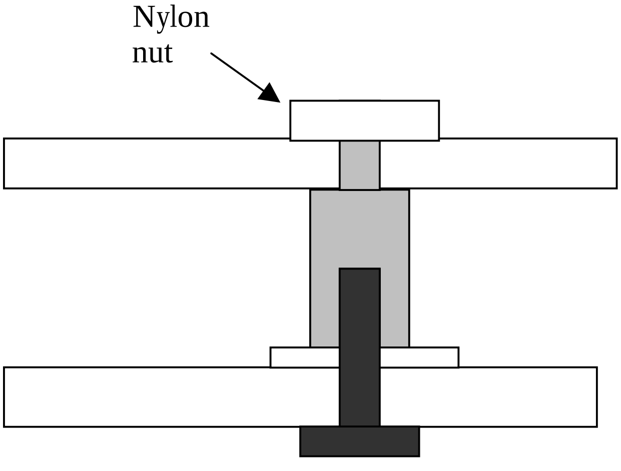
The HERON module carriers are fitted with four fixing pillars with 5mm bodies, and a female end and a male end. i.e



These are fitted to the carrier board using an M3 nylon bolt from the non module side of the carrier, and there is a nylon washer fitted between the metal pillar and the module side surface of the PCB. i.e.



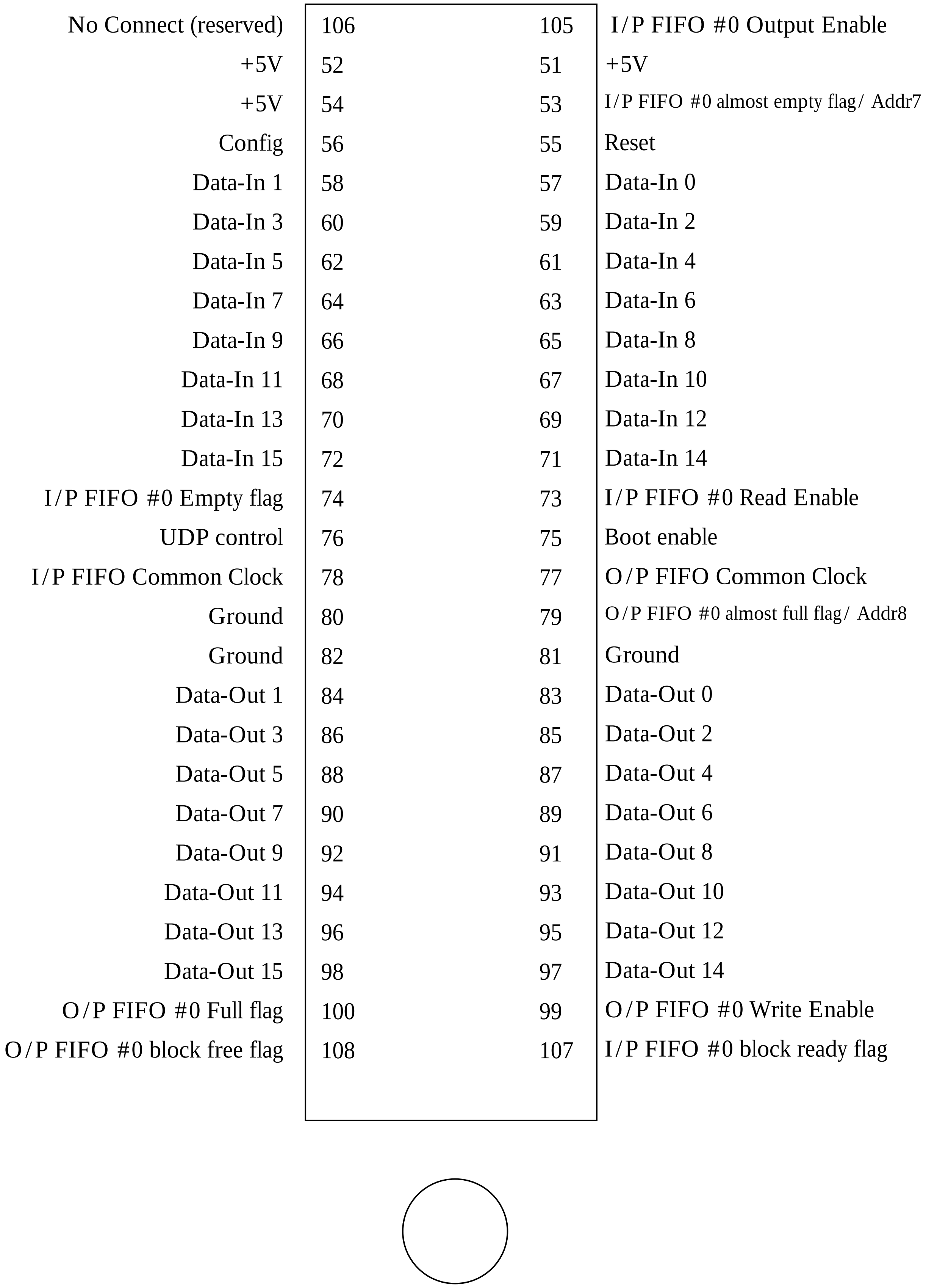
This means that when the HERON modules are fitted, the male part of the pillars helps to properly align the module as it is pushed into the sockets. Then an M3 nylon nut can be fitted to the top of the module to firmly retain it in each of four places.



HERON module Connector Pinout

** shows changes from GDIO pin function

Serial Bus Data	102	101	Serial Bus Clock
+5V	2	1	Module detect **
+5V	4	3	Module has serial bus**
+5V	6	5	Ground
+5V	8	7	Ground
**I/P FIFO #0 Def0	10	9	Ground
**I/P FIFO #0 Def1	12	11	Polarisation
**I/P FIFO #0 Def2	14	13	Ground
**I/P FIFO #0 Def3	16	15	Ground
**I/P FIFO #0 Def4	18	17	Ground
**I/P FIFO #0 Def5	20	19	Ground
**O/P FIFO #0 Def0	22	21	Ground
-12V	24	23	Ground
-12V	26	25	-12V
-12V	28	27	Ground
-12V	30	29	Ground
**O/P FIFO #0 Def1	32	31	Ground
**O/P FIFO #0 Def2	34	33	Ground
**O/P FIFO #0 Def3	36	35	Ground
**O/P FIFO #0 Def4	38	37	Ground
Polarisation	40	39	Ground
**O/P FIFO #0 Def5	42	41	Ground
+12V	44	43	Ground
+12V	46	45	+12V
+12V	48	47	Ground
+12V	50	49	Ground
No Connect (reserved)	104	103	Module has processor



No Connect (reserved)	106	105	I/P FIFO #0 Output Enable
+5V	52	51	+5V
+5V	54	53	I/P FIFO #0 almost empty flag/ Addr7
Config	56	55	Reset
Data-In 1	58	57	Data-In 0
Data-In 3	60	59	Data-In 2
Data-In 5	62	61	Data-In 4
Data-In 7	64	63	Data-In 6
Data-In 9	66	65	Data-In 8
Data-In 11	68	67	Data-In 10
Data-In 13	70	69	Data-In 12
Data-In 15	72	71	Data-In 14
I/P FIFO #0 Empty flag	74	73	I/P FIFO #0 Read Enable
UDP control	76	75	Boot enable
I/P FIFO Common Clock	78	77	O/P FIFO Common Clock
Ground	80	79	O/P FIFO #0 almost full flag/ Addr8
Ground	82	81	Ground
Data-Out 1	84	83	Data-Out 0
Data-Out 3	86	85	Data-Out 2
Data-Out 5	88	87	Data-Out 4
Data-Out 7	90	89	Data-Out 6
Data-Out 9	92	91	Data-Out 8
Data-Out 11	94	93	Data-Out 10
Data-Out 13	96	95	Data-Out 12
Data-Out 15	98	97	Data-Out 14
O/P FIFO #0 Full flag	100	99	O/P FIFO #0 Write Enable
O/P FIFO #0 block free flag	108	107	I/P FIFO #0 block ready flag

I/P FIFO #1 Read Enable	110	109	O/P FIFO #1 Write Enable
I/P FIFO #2 Read Enable	112	111	O/P FIFO #2 Write Enable
I/P FIFO #3 Read Enable	114	113	O/P FIFO #3 Write Enable
I/P FIFO #4 Read Enable	116	115	O/P FIFO #4 Write Enable
I/P FIFO #5 Read Enable	118	117	O/P FIFO #5 Write Enable
I/P FIFO #1 Empty flag	120	119	O/P FIFO #1 Full flag
I/P FIFO #2 Empty flag	122	121	O/P FIFO #2 Full flag
I/P FIFO #3 Empty flag	124	123	O/P FIFO #3 Full flag
I/P FIFO #4 Empty flag	126	125	O/P FIFO #4 Full flag
I/P FIFO #5 Empty flag	128	127	O/P FIFO #5 Full flag
I/P FIFO #1 almost Empty flag/ Addr9	130	129	O/P FIFO #1 almost full flag/ Addr10
I/P FIFO #2 almost Empty flag/ Addr11	132	131	O/P FIFO #2 almost full flag/ Addr12
I/P FIFO #3 almost Empty flag/ Addr13	134	133	O/P FIFO #3 almost full flag/ Addr14
I/P FIFO #4 almost Empty flag/ Addr15	136	135	O/P FIFO #4 almost full flag/ Addr16
I/P FIFO #5 almost Empty flag/ Addr17	138	137	O/P FIFO #5 almost full flag/ reserved
I/P FIFO #1 block ready flag	140	139	O/P FIFO #1 block free flag
I/P FIFO #2 block ready flag	142	141	O/P FIFO #2 block free flag
I/P FIFO #3 block ready flag	144	143	O/P FIFO #3 block free flag
I/P FIFO #4 block ready flag	146	145	O/P FIFO #4 block free flag
I/P FIFO #5 block ready flag	148	147	O/P FIFO #5 block free flag
I/P FIFO #1 Output Enable	150	149	I/P FIFO #2 Output Enable
I/P FIFO #3 Output Enable	152	151	I/P FIFO #4 Output Enable
I/P FIFO #5 Output Enable	154	153	Addr/Flagsel
JTAG TMS	156	155	JTAG TCK
JTAG EMU0	158	157	JTAG TDI
JTAG EMU1	160	159	JTAG TDO
JTAG presence detect	162	161	JTAG TRST

Data-In 17	164	163	Data-In 16
Data-In 19	166	165	Data-In 18
Data-In 21	168	167	Data-In 20
Data-In 23	170	169	Data-In 22
Data-In 25	172	171	Data-In 24
Data-In 27	174	173	Data-In 26
Data-In 29	176	175	Data-In 28
Data-In 31	178	177	Data-In 30
Module interconnect 0	180	179	Addr0
Module interconnect 1	182	181	Addr1
Module interconnect 2	184	183	Addr2
Module interconnect 3	186	185	Addr3
32/16 select	188	187	Addr4
Data-Out 17	190	189	Data-Out 16
Data-Out 19	192	191	Data-Out 18
Data-Out 21	194	193	Data-Out 20
Data-Out 23	196	195	Data-Out 22
Data-Out 25	198	197	Data-Out 24
Data-Out 27	200	199	Data-Out 26
Data-Out 29	202	201	Data-Out 28
Data-Out 31	204	203	Data-Out 30
Periphrd	206	205	Periphwr
Module ID0	208	207	Carrier ID0
Module ID1	210	209	Carrier ID1
Module ID2	212	211	Carrier ID2
Module ID3	214	213	Carrier ID3
Addr5	216	215	Addr6

Notes:

1. The original Synchronous GDIO pin-out has been modified in only three respects,

a) The module detect pin. A module carrier can now pull up this previously GND pin with a 10K resistor, so that a high level shows no module is fitted. No change is needed to the modules, this pin should still be grounded.

b) The FIFO #0 defn bits. These are used to allow a module to easily specify routing of FIFO0 data, without having to perform the full register write sequence. It is primarily intended to simplify the support of legacy modules, but could also be used in new designs, where full programmability is not necessary. The Module Carrier board will pull these signals high with a 10K resistor. The coding can thus be easily accomplished by fitting a shorting link between the relevant bit(s) and the adjacent ground pin on the same connector. The complete definition of these bits is left to the Carrier board, so they could have different functions on different carrier boards. Hence it is recommended that these are either set by links, or in software by the user, allowing the correct setting to be made depending on the carrier board used.

c) The Module has serial bus pin. A module carrier can now pull up this previously GND pin with a 10K resistor, so that a high level shows the module implements the serial bus. No change is needed to legacy modules, this pin should still be grounded. This is also the case for new modules that do not use the serial bus.

2. The signals for providing the 32-bit interface are all on the new “bottom” connector, allowing 32-bit modules to be made by just adding this connector and not the fourth. The only limit is the number of FIFO channels that can be used, but an I/O device will probably only require one input and one output anyway.

3. The 32/16 bit select is pulled up on the carrier board, and a high level shows a 16-bit interface, so a module with only two connectors will operate automatically in 16-bit mode. A 32-bit module must drive this pin low.

4. The JTAG presence detect signal is pulled up by the carrier board, and a high level on this shows no module present, or JTAG not used on this module. When this signal is high, the carrier board automatically connects the TDI to TDO pins of the module. A module that connects to the JTAG chain must drive this pin low.

Power

Signal name	**Driven by**	**Description**
GND	Carrier	System Ground
+5V	Carrier	System +5 Volts, 4 A maximum rating of the connector
-12V	Carrier	System –12 Volts, 4 A maximum rating of the connector
+12V	Carrier	System +12 Volts, 4 A maximum rating of the connector

Any other voltages required by the module circuitry must be generated on the module.

Signal voltage levels

Early HERON module carriers like the HEPC8 used 5V TTL logic, but even early module types actually used 3.3V "LVTTL" signals that achieve logic levels compatible with 5V TTL, and are themselves 5V tolerant.

As technology progresses more and more logic that might be used on a module uses low voltage signal levels, not all of which are 5V tolerant.

So at revision A of this specification (the first fully released version) a decision has been taken that new HERON Module carriers shall use 3.3V signal levels at the HERON module pins, but that the carrier board shall tolerant of 5V signals driven from a module. This allows the use of 5V modules, and 3.3V modules that need not be 5V tolerant.

It is recognised that it might eventually be desirable to use even lower logic levels, but that will be addressed when it arises.

Miscellaneous signals

Signal name	**Driven by**	**Description**
No Connect (reserved)	None	Unused in this version of the specification leave unconnected.
Polarisation	None	Protection against incorrect module insertion. Carrier board has this connector receptacle blanked, Module has this pin removed from the connector.
Module detect	Module	Carrier pulls this signal high using 10K. Module connects this pin to ground, thus a Carrier board can detect the presence of a module by a low logic level on this pin.

Module has processor	Module	Carrier pulls this signal high using 10K. A module that has a processor, connects this pin to ground, thus a Carrier board can detect the difference between a processor module, and an I/O module. If the Module detect signal is low, then a low logic level on this pin shows the module has a processor.
Module has serial bus	Module	Carrier pulls this signal high using 10K. If a module does not implement the serial configuration bus, it connects this pin to ground, thus a Carrier board can detect the absence of a serial bus by a low logic level on this pin.
Module ID(0..3)	Carrier	The carrier asserts a binary encoded module ID onto these pins to allow the module to uniquely identify itself on this carrier. Signal is 5V or 0V
Carrier ID(0..3)	Carrier	The carrier asserts a binary encoded Carrier ID onto these pins to allow the module to uniquely identify which carrier in the system it is fitted to. Signal is +5v or 0v
Uncommitted Module interconnect(0..3)	Module	The carrier simply busses these pins together across all of the module slots on this board. These are application specific connections, as and when supported by the combination of modules fitted. A module carrier will pull these signals high with 10K. Examples are:- 1.Programmable clocks being passed from a processor timer pin to an I/O module 2. I/O modules asserting a processor interrupt on another module.
Addr/flagsel	Carrier	This pin is driven high by a module carrier if the flag/addr pins are connected to FIFO flags, if the pins are used to address Carrier card peripherals the carrier drives this pin low.
32/16 select	Module	A Carrier pulls this signal high using a 10K. If a module is designed to use the 32 bit mode it must drive this pin low, so that the Carrier board interface logic can use this signal to select between 32 bit operation (this signal low) and 16 bit operation (this signal high).

Detect pins

The "Module detect", "Module has processor" and "Module has serial bus" pins are provided to allow Carrier card logic to make some assessment of the type of module fitted.

Some carriers might allow the host computer to read these pins in order to make some automatic checking of configurations, however, the exact use of these pins might vary between different carrier card designs.

ID pins

The Module and Carrier ID pins are so that a module can always be addressed uniquely in a system. This information can be used for boot selection, or other features as defined by the individual module or software tool specification. The Carrier is expected to have a switch that allows the user to set the carrier ID, and to assign unique Module IDs to each module slot. Other devices on the carrier such as host interfaces, or board to board connections may also be assigned module IDs to allow them to be addressed uniquely as well.

It is expected that some software tools will use a broadcast boot stream. In this case the combination of the Carrier ID and Module ID can be used to ignore all parts of the boot stream not intended for this module.

These pins are also involved when addressing modules over the serial configuration bus.

Uncommitted Module Interconnect pins

The module interconnect pins are simply bussed between modules by the carrier. They can be used to connect signals directly between modules. Examples may be to allow I/O modules to directly interrupt processors, or perhaps to allow a processor to provide a programmable clock for an I/O device.

Addr/flagsel pin

This pin is driven by the Carrier board, and is intended to allow some HERON module slots to gain access to more direct address range, when required by that particular module slot in that board. Usually the Module would only need a small address reach to allow it to initialise some control registers. In this case the Carrier card will drive the “Addr/flagsel” pin high, and will connect the “almost flags” from the FIFO to the shared pins.

However if an OEM board, or a particular module slot of a carrier card, has a special function that requires more address reach, the Carrier card can drive this pin low, and assume the shared pins are driven as address pins.

So if a processor module uses this pin to enable some address lines onto these pins, it is possible for the same processor module design to be used in both ways.

The loss of the FIFO “Almost flags” does not lose any connectivity to the FIFOS, but merely reduces the possibility to use smaller DMA sizes. The almost flags are really intended for use by a hardware module rather than a Processor module, (see section on use of FIFO flags). Any module slot that was designed to use extended addressing would require a processor module anyway, so the loss of the almost flags is unimportant.

Of course a Carrier card in either mode can achieve larger address reach, by using paging techniques.

32/16 select pin

This pin is provided so that the Carrier card can automatically detect the difference between a module that uses the legacy 16 bit mode, and one that uses the 32 bit mode.

The Carrier card should automatically switch modes depending on the state of this pin.

FIFO signals

N.B. where the terminology "high" is used this means +3.3V

Signal name	**Driven by**	**Description**
Data_in(0..15)	Carrier	This is the input FIFO data. It is for data passing from the carrier board to the module. These are the low 16 bits as used by 16 or 32 bit module variants. These bits are also used when reading from Carrier board configuration registers, which is only possible from a 32 bit module.
Data_in(16..31)	Carrier	This is the input FIFO data. It is for data passing from the carrier board to the module. These are the high 16 bits which are only used by 32 bit module variants. These bits are also used when reading from Carrier board configuration registers, which is only possible from a 32 bit module.
Data_out(0..15)	Module	This is the output FIFO data. It is for data passing from the module to the carrier board. These are the low 16 bits as used by 16 or 32 bit module variants. These bits are also used when writing to Carrier board configuration registers, which is only possible from a 32-bit module.
Data_out(16..31)	Module	This is the output FIFO data. It is for data passing from the module to the carrier board. These are the high 16 bits which are only used by 32 bit module variants. These bits are also used when writing to Carrier board configuration registers, which is only possible from a 32-bit module.
I/P FIFO Common clock	Module	This is the clock that is used to clock all of the Input FIFOs for this module. It must be driven by the module with at least 45mA so that it can drive a parallel 220/330R termination on the carrier board.
O/P FIFO Common clock	Module	This is the clock that is used to clock all of the Output FIFOs for this module. It must be driven by the module with at least 45mA so that it can drive a parallel 220/330R termination on the carrier board.
I/P FIFO #n read enable	Module	These read enable signals are used to perform a read from the input FIFO designated by n. (refer to FIFO signal definitions for details)

O/P FIFO #n write enable	Module	These write enable signals are used to perform a write to an O/P FIFO designated by n. (refer to FIFO signal definitions for details)
I/P FIFO #n Output enable	Module	These output enables are used to select which I/P FIFO (if any) is driving the I/P FIFO data pins. If a peripheral access to the carrier board is made, all of the FIFO output enables must be high (not asserted). In order for a 16 bit I/O module to gain access to FIFO #0, the I/P FIFO #0 Output enable signal; is pulled low by the carrier card, while the others are pulled high.
I/P FIFO #(0..5) Empty flag.	Carrier	This flag is driven by the relevant FIFO to indicate that it is empty and no more data can be read. (refer to FIFO signal definitions for details)
I/P FIFO #(0..5) Almost Empty flag /Addrn	Carrier	When the Addr/flagsel pin is high:- This flag is driven by the relevant FIFO to indicate that it is almost empty and more data can only be read after inspecting the relevant empty flag. (refer to FIFO signal definitions for details) N.B. It should not be necessary for the number of data items left to be known for correct operation. In fact there will always be four 32-bit data items left in the FIFO, but in some carrier board implementations there might be more.
I/P FIFO #(0..5) block ready flag	Carrier	This flag is driven by the relevant FIFO to indicate that it has a block ready for reading by the module. (refer to FIFO signal definitions for details) N.B. It should not be necessary for the number of data items in the block to be known for correct operation. In fact this flag will indicate that at least 32, 32-bit data items left in the FIFO, but in some carrier board implementations there might be more.
O/P FIFO #(0..5) Full flag.	Carrier	This flag is driven by the relevant FIFO to indicate that it is full and no more data can be written. (refer to FIFO signal definitions for details)
O/P FIFO #(0..5) Almost Full flag /Addrn	Carrier	When the Addr/flagsel pin is high:- This flag is driven by the relevant FIFO to indicate that it is almost Full and more data can only be written after inspecting the relevant full flag. (refer to FIFO signal definitions for details) N.B. It should not be necessary for the amount of space left to be known for correct operation. In fact there will always be four 32-bit spaces left in the FIFO, but in some carrier board implementations there might be more.

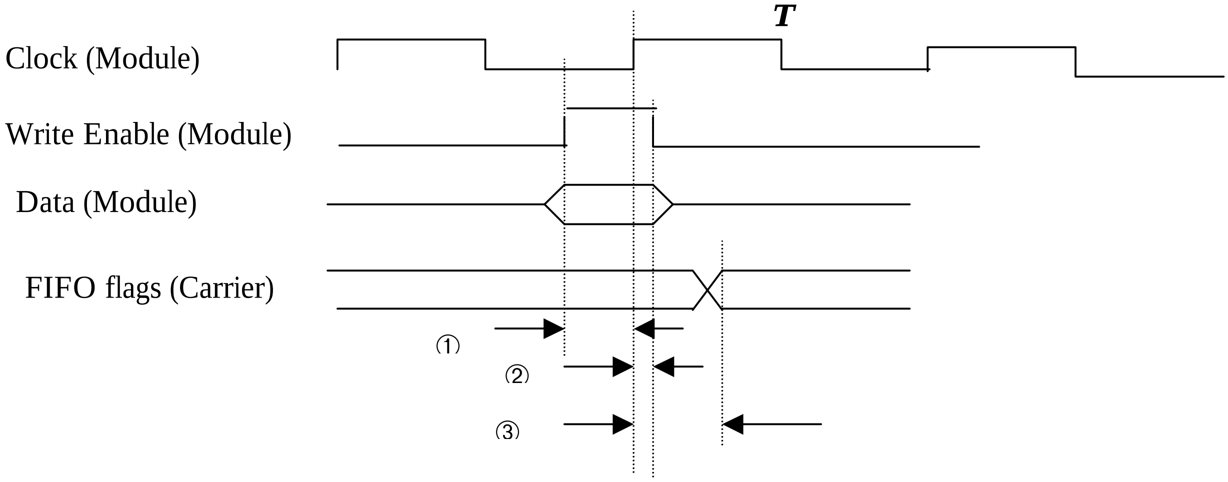
O/P FIFO #(0..5) block free flag	Carrier	This flag is driven by the relevant FIFO to indicate that it has a block of space free for writing by the module. (refer to FIFO signal definitions for details) N.B. It should not be necessary for the number of data items in the block to be known for correct operation. In fact this flag will indicate that at least 32, 32-bit spaces left in the FIFO, but in some carrier board implementations there might be more.
I/P FIFO #0 Def(0..5)	Module	The module uses these bits to pass some routing information to the carrier card, without having to perform the full register write sequence. It is provided mainly so that simple I/O cards like the legacy GDIO modules can set-up some default routing for the data from the Carrier card communications system, into I/P FIFO#0. The exact implementation of these bits is dependent on the Carrier board design, so they should be settable by user jumpers.
O/P FIFO #0 Def(0..5)	Module	The module uses these bits to pass some routing information to the carrier card, without having to perform the full register write sequence. It is provided mainly so that simple I/O cards like the legacy GDIO modules can set-up some default routing for the data from O/P FIFO#0 to the Carrier card communications system. The exact implementation of these bits is dependent on the Carrier board design, so they should be settable by user jumpers.

The FIFO interfaces are all identical, so we only need describe one of them. All FIFO interfaces implemented by a Module Carrier must conform to this timing.

The FIFOs in both directions are synchronous, and the Module provides the clocks so the data rate can be set by the requirements of the module.

FIFO Write

The basic timing for a write cycle is



There will be faster versions of the FIFO interface over time, but the initial interface will have a maximum clock frequency of 67Mhz. As faster interfaces are implemented this document will be updated with the timings used by them, it is however expected that a slower module will always be able to work with the timings of a faster Carrier card.

In reality this might not always be the case, for example there may be some modules designed for 67Mhz module slots that drive their FIFO clock at less than 62.5Mhz. In that case they will not work in a 100Mhz module slot without modification.

67Mhz

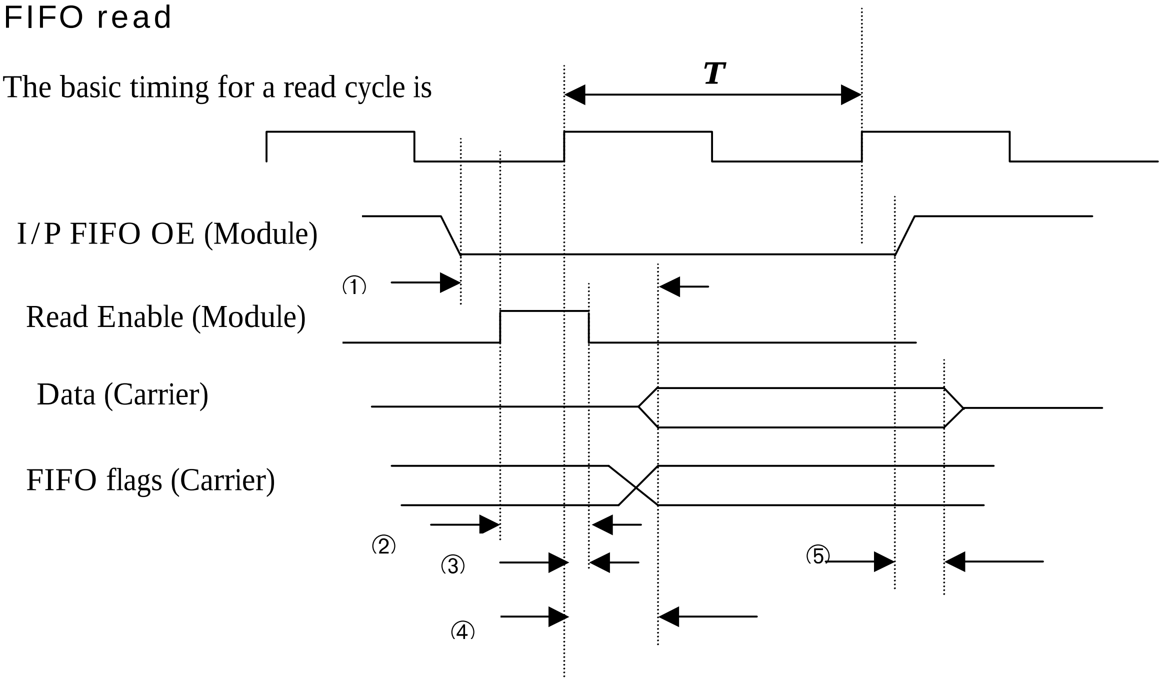
	Description	Min (ns)	Max (ns)
Tclkl	Clock low time	6	
Tclkh	Clock high time	6	
①	Data and Write Enable set up before Clk ↑	8	
②	Data and Write Enable hold after Clk ↑	1	
③	Delay to FIFO flag valid after Clk ↑	2	10

100MHz

	Description	Min (ns)	Max (ns)
Tclkl	Clock low time	2.4	
Tclkh	Clock high time	2.4	
T	Clock period	10 (F=100Mhz)	16.66 (F=60Mhz)
δT	Clock period tolerance	-1.0	+1.0
εT	Clock Jitter	-0.15	+0.15
①	Data and Write Enable set up before Clk ↑	5.0	
②	Data and Write Enable hold after Clk ↑	0	
③	Delay to FIFO flag valid after Clk ↑	1.5	7.2

FIFO read

The basic timing for a read cycle is



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In reality this might not always be the case, for example there may be some modules designed for 67Mhz module slots that drive their FIFO clock at less than 62.5Mhz. In that case they will not work in a 100Mhz module slot without modification.

67Mhz

	Description	Min (ns)	Max (ns)
Tclkl	Clock low time	6	
Tclkh	Clock high time	6	
①	I/P FIFO Output Enable low to data driven	8	
②	Read Enable set up before Clk ↑	8	
③	Read Enable hold after Clk ↑	1	
④	Delay to data and FIFO flags valid after Clk ↑	2	11
⑤	I/P FIFO Output Enable high to data tri-state	0	6

100MHz

	Description	Min (ns)	Max (ns)
Tclkl	Clock low time	2.4	
Tclkh	Clock high time	2.4	
T	Clock period	10 (F=100Mhz)	16.66 (F=60Mhz)
δT	Clock period tolerance	-1.0	+1.0
εT	Clock Jitter	-0.15	+0.15
①	I/P FIFO Output Enable low to data driven	0	9.0
②	Read Enable set up before Clk ↑	6.2	

③	Read Enable hold after Clk ↑	0	
④	Delay to data and FIFO flags valid after Clk ↑	1.5	7.2
⑤	I/P FIFO Output Enable high to data tri-state	0	9.0

FIFO flags

All of the FIFO flags are active low - that is asserted when low.

The Full, Almost Full and Block free flags are synchronised to the Write Clock with the timing shown.

The Empty, Almost Empty and Block ready flags are synchronised to the Read Clock with the timing shown.

The FIFOs on HERON carriers operate in “normal” mode, as opposed to “first word fall through” mode. That is the flags are truly Empty and Full flags not Input ready (IR) and Output ready (OR) flags.

The intended use of FIFO flags

There are three different flags from each FIFO provided by the HERON module connectors.

These are

1. The Full/Empty flags, which indicate if a transfer of size 1 can take place.
2. The “Almost” flags that indicate that the FIFO end is near.
3. The “Block” flags that indicate a block transfer can happen.

These three types are provided to cover a wide range of needs. It is intended that these needs split into two main types, Processor based modules, and Hardware based modules.

The Processor based modules will strive to use DMA to transfer data to and from the FIFOs, so data will be better transferred in large blocks. This is why the “Block” fags are provided – to trigger DMA transfers. However data will not always be transferred in integers of this block size, so the Full/Empty flag is needed to transfer the small number left after the blocks are done. This means that processor based modules will normally connect only to the Block and Full/Empty flags.

Hardware based modules however will transfer objects one at a time probably using some type of synchronous state machine. This means it could be possible to make FIFO accesses on consecutive clocks by driving the enable signal for several clock cycles. The timing of the flags however make it likely that the flag indicating the end of the transfer, will occur after the next transfer is already started. In this case using the Full/Empty flags is impossible, but transferring on consecutive clocks until the “Almost” flag is received means that the extra cycle does not overrun the end of the FIFO. If necessary the final few transfers can be made by the state machine “one at a time” inspecting the Full/Empty flag after each cycle. This means that the hardware modules will normally only connect to the “Almost” and Full/Empty flags.

System control signals

N.B. any reference to “high” means +3.3V

Signal name	**Driven by**	**Description**
Reset	Carrier	System reset signal asserted low to perform a reset.
Config	Either	This signal is an open collector signal that is connected only on this Carrier board. It is pulled high using a 100R on the carrier, and is driven low by a processor module upon reset. Software on each processor module will release the drive from this signal after it is booted. I/O modules that are not providing a boot stream can therefore be disabled while this signal is low.
UDP control	Module	This allows certain I/O modules to be used to propagate a reset signal from a remote board. This output can be driven low to assert a reset of this carrier board. NB a jumper setting on the carrier board might be required in order to use this option.
Boot enable	Module	This can be used to override the blocking caused by the assertion of the Config signal. This signal must be pulled high using 10K on the carrier board. If this signal is high the flow of data is blocked until the Config signal is released, if it is low, data is allowed to flow regardless of the state of the Config signal.

JTAG (IEEE 1148.1) signals

N.B. all signals are 3.3V level signals

Signal name	**Driven by**	**Description**
JTAG presence detect	Module	The carrier card pulls this signal high with a 10K. A module that connects to the JTAG chain must pull this signal low to GND to show that it will connect to TDI and TDO. Otherwise the JTAG chain will be “self healed” by the carrier card.
JTAG TMS	Carrier	The JTAG test mode select
JTAG TCK	Carrier	The JTAG clock signal
JTAG TDI	Carrier	The input of the serial scan path to the module
JTAG TDO	Module	The output of the serial scan path from the module
JTAG TRST	Carrier	The JTAG reset signal
JTAG EMU(0..1)	Module	These signals are bussed between modules on the carrier card, and processors can be programmed to drive one of these signals when a breakpoint is reached. Other processors can then be programmed to breakpoint when this signal is asserted. This can thus be used for simultaneous breakpointing of multiple processors on a board. These signals are not connected between boards.

JTAG Presence detect

The JTAG presence detect must be used by a HERON carrier to drive the enable pin of a buffer. This device must be used to connect the TDI directly to the TDO of a slot that does not have a module, or whose module does not implement the JTAG chain. Suitable logic technology must be chosen to ensure near zero delay though this device.

Heron Serial Bus

Signal name	**Driven by**	**Description**
Serial bus data	Either	HSB data line
Serial bus clock	Either	HSB clock line

This bus is provided so any other member of the bus can configure those I/O modules that provide this feature. This could be the host interface or a processor module. The use of this slow serial bus is preferable for such configuration information to the use of a high bandwidth communications channel.

Any module that implements this serial bus will obey some basic rules as regards addressing, and will return some unique information that could allow configuration software to determine the exact module type fitted to any module socket.

This serial bus is not compulsory, but it is assumed that as the HERON module range matures more and more modules will implement it, making some auto-configuration tools possible.

The exact definition of the protocol on this bus is defined in the separate “Heron Serial Bus Specification” document.

Carrier card peripheral access

Signal name	Driven by	Description
Addr[0..6]	Module	Address bits to be used to address carrier board peripherals. These bits for the address of 32 bit words.
I/P FIFO#n almost flag/ Addrm	Module	When the Addr/flagsel pin is low:- These pins form the upper address bits used to access carrier card peripherals, expanding the address reach. N.B. A Carrier card that uses these pins as address bits, i..e. pulls the Addr/flagsel pin low, AND has the FIFO connections, must allow access to the block flags via a register in the peripheral access space.
Periphwr	Module	Asynchronous Carrier card peripheral write pin
Periphrd	Module	Asynchronous Carrier card peripheral read pin

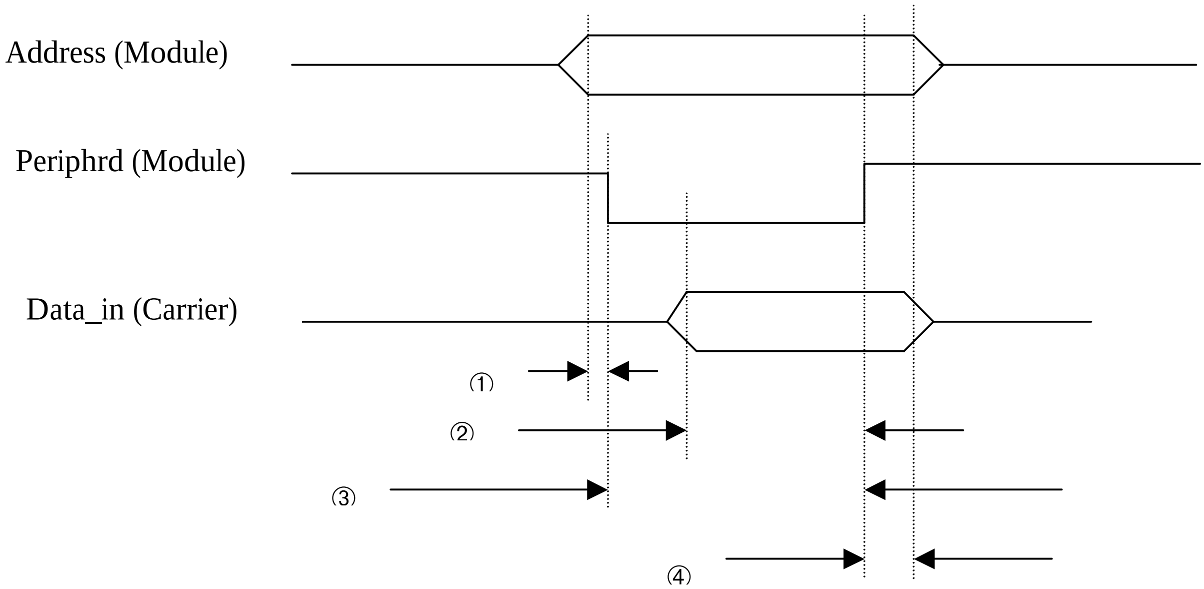
This interface is provided to allow modules to perform direct accesses to Carrier card peripherals. The exact definition of the peripherals will vary from carrier card to carrier card, and perhaps even from module slot to module slot on the same carrier.

For this reason it is expected that Processor modules simply allow software to access these peripherals, and then the user can program the system to correctly access the carrier peripherals.

It is hoped that when the serial bus protocol definition is completed, that there is a method for accessing at least a subset of these peripherals via that serial bus. In this way a processor module in another slot can configure the Carrier card peripherals of a slot occupied by an I/O module.

The interface is a simple asynchronous one, using the address bits combined with the assertion of a read signal to access data from the Carrier card peripherals via the Data-In pins. Likewise the use of the address bits combined with a write signal can write data to the Carrier card peripherals via the Data-out pins.

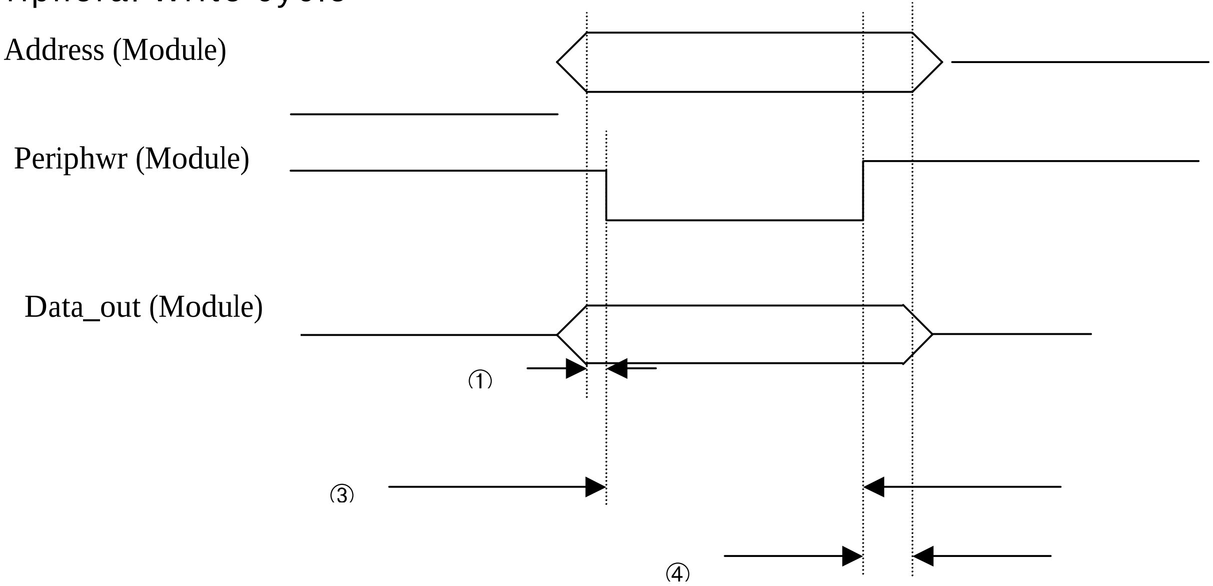
Peripheral Read cycle



	Description	Min (ns)	Max (ns)
①	Address set-up to Periphrd ↓	2	
②	Data set-up to Periphrd ↑	25	
③	Periphrd pulse length	30	
④	Data and address hold after Periphrd ↑	2	

This timing definition is the same for the 67Mhz and 100Mhz carrier variants, as it is actually a definition of what the Modules will expect of a carrier. A particular module design may in fact have a periphd pulse length longer than that specified, but not shorter. If a carrier requires the periphrd pulse length to be extended, this can be achieved with a different setting of the bus control register of that module.

Peripheral Write cycle

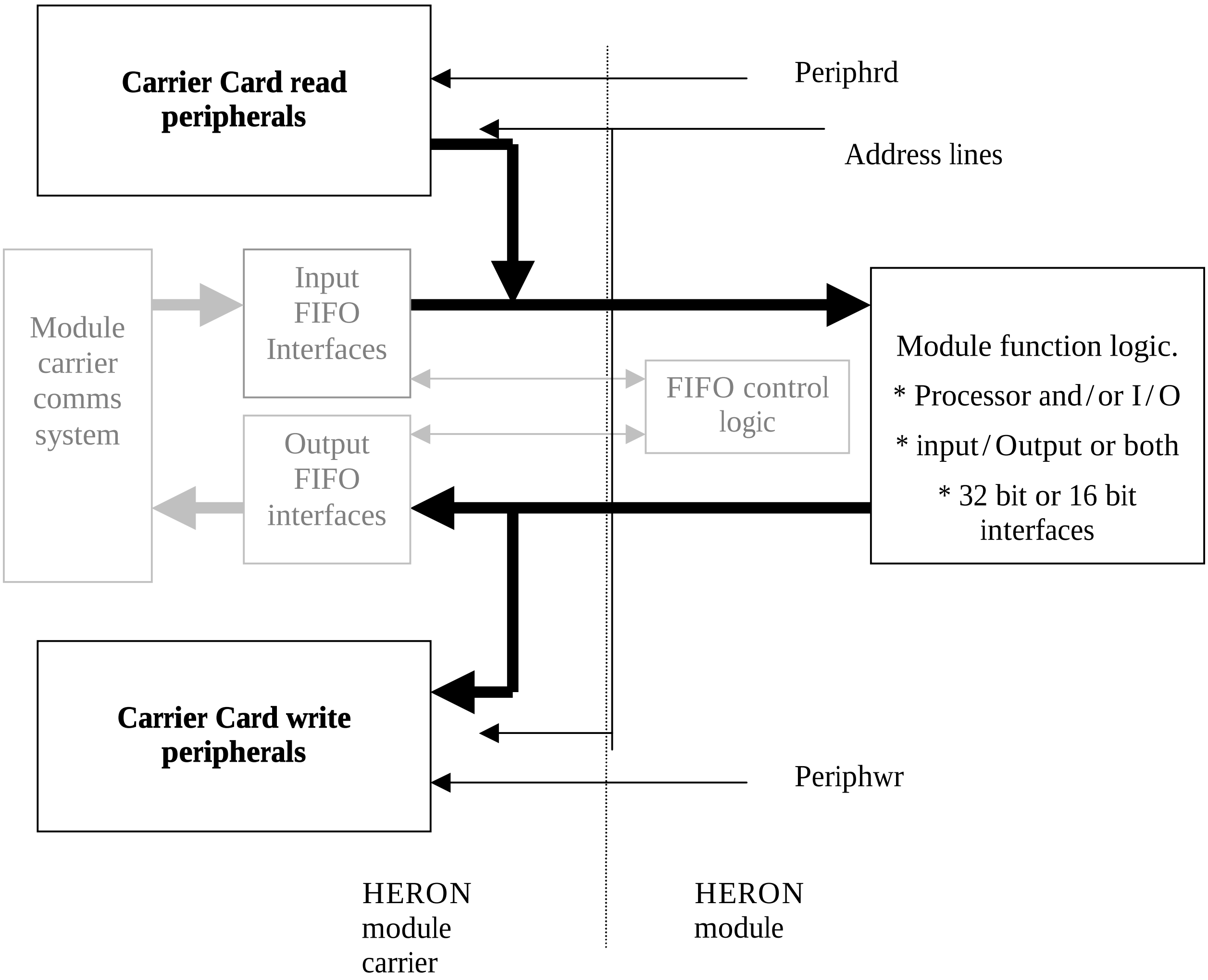


	Description	Min (ns)	Max (ns)
①	Address and data set-up to Periphwr ↓	2	
③	Periphwr pulse length	30	
④	Data and address hold after Periphwr ↑	2	

This timing definition is the same for the 67Mhz and 100Mhz carrier variants, as it is actually a definition of what the Modules will provide to a carrier. A particular module design may in fact have a peripwr pulse length longer than that specified, but not shorter. If a carrier requires the periphwr pulse length to be extended, this can be achieved with a different setting of the bus control register of that module.

Example of the use of the peripheral interface

The interface between a carrier card peripheral and the HERON module is deliberately made very simple, and used the minimum of signals.



The diagram demonstrates the sharing of the HERON module data busses with the FIFO interfaces. This means that the peripheral accesses cannot take place at the same time as the FIFO accesses. Please note that to perform a peripheral read cycle the FIFO output enables must be inactive to prevent the FIFOs from driving the module's input data bus.

The diagram also shows the use of a single control signal to make a read access and another single control signal to make the write access. There is no involvement of the other signals such as clocks.

The module always drives the address bits Addr[0..6] for use in peripheral access cycles. If the carier card requires more address reach, the module can provide Addr[7..19] on the pins normally used for the FIFO "almost" flags. The carrier card selects the mode of these pins, by driving the addr/flagsel pin. This pin is normally driven high by the carrier, and the shared pins used as FIFO flags, but a carrier that requires the extra address lines can pull this pin low.

Data ordering with a 16-bit module

Even when a 16-bit module is implemented, transmitting and receiving data must happen in complete 32-bit words.

When the Module Carrier board FIFO has data for the module, the data is split into two 16 bit half words for sending to the 16-bit module. The first half word to be received by the 16-bit module will be the bottom half of the 32-bit word and the second 16 bits will be the top half of the 32-bit word.

The following example demonstrates this operation.

1st 32 bit Word in the FIFO = 0x04030201

2nd 32 bit Word in the FIFO = 0x08070605

1st half word read by the 16-bit module is 0x0201

2nd half word read by the 16-bit module is 0x0403

3rd half word read by the 16-bit module is 0x0605

4th half word read by the 16-bit module is 0x0807

When the 16-bit module writes to the FIFO on the Module Carrier card, the same ordering applies. The first 16-bit data written will form the bottom 16 bits of the 32-bit word in the FIFO. The second 16-bit data written will form the top 16 bits of the 32-bit word in the FIFO.

The following example demonstrates this operation.

1st half word written by the 16-bit module is 0x0201

2nd half word written by the 16-bit module is 0x0403

3rd half word written by the 16-bit module is 0x0605

4th half word written by the 16-bit module is 0x0807

1st 32 bit Word in the FIFO = 0x04030201

2nd 32 bit Word in the FIFO = 0x08070605

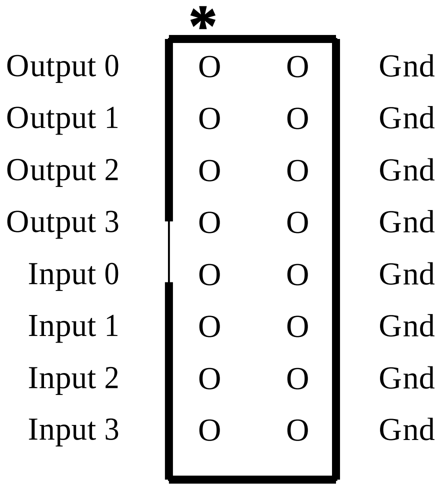
Digital I/O connector

The HERON processor modules manufactured by HUNT ENGINEERING will provide some simple digital I/O (4 bits in and 4 bits out). This digital I/O is not part of the HERON specification, and is usually configured for use via a cable plugged into the top of the module. However we have chosen a 2mm pitch connector that has a PCB footprint like that of the HERON module connectors. All HUNT ENGINEERING processor modules that implement this digital I/O will place the connector in the same position of the module, allowing OEMs to use a Carrier card connector in this position if preferred. In that case the OEM could request that modules supplied to them by HUNT ENGINEERING are fitted with the correct connectors to mate with those carrier card connectors.

The Connectors used on the HUNT ENGINEERING module are :-

Shrouded right angle connector with a 2mm pitch. It is supplied by Molex and its part number is 87333-1620.

Their pinout is



Output 0	O	O	Gnd
Output 1	O	O	Gnd
Output 2	O	O	Gnd
Output 3	O	O	Gnd
Input 0	O	O	Gnd
Input 1	O	O	Gnd
Input 2	O	O	Gnd
Input 3	O	O	Gnd

This side of the right angle connector is the side against the PCB of the HUNT ENGINEERING C6000 HERON modules

Their position on the module is shown at the end of this section, along with the position of the McBSP connectors.

If a carrier card connector is used its part number should be:-

Samtec SMM-108-01-S-D

In which case HUNT ENGINEERING will fit the mating half (part number) on request.

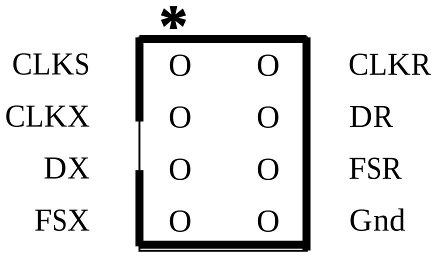
Samtec TMM-108-03-G-D

Serial port connector

The HERON C6000 processor modules manufactured by HUNT ENGINEERING will provide a connection to the ‘C6000 Multi-Channel Buffered serial port McBSP. These serial ports are not part of the HERON specification, and are usually configured for use via a cable plugged into the top of the module. However we have chosen a 2mm pitch connector that has a PCB footprint like that of the HERON module connectors. All HUNT ENGINEERING C6000 processor modules that implement this McBSPs will place the connector in the same position of the module, allowing OEMs to use a Carrier card connector in this position if preferred. In that case the OEM could request that modules supplied to them by HUNT ENGINEERING are fitted with the correct connectors to mate with those carrier card connectors.

The Connectors used on the HUNT ENGINEERING module are shrouded right angle connector with a 2mm pitch. It is supplied by Molex and its part number is 87333-0820.

Their pinout is



This side of the right angle connector is the side against the PCB of the HUNT ENGINEERING C6000 HERON modules

Their position on the module is shown at the end of this section, along with the position of the McBSP connectors.

If a carrier card connector is used its parts number should be:-

Samtec SMM-108-01-S-D

In which case HUNT ENGINEERING will fit the mating half (part number) on request.

Samtec TMM-104-03-G-D

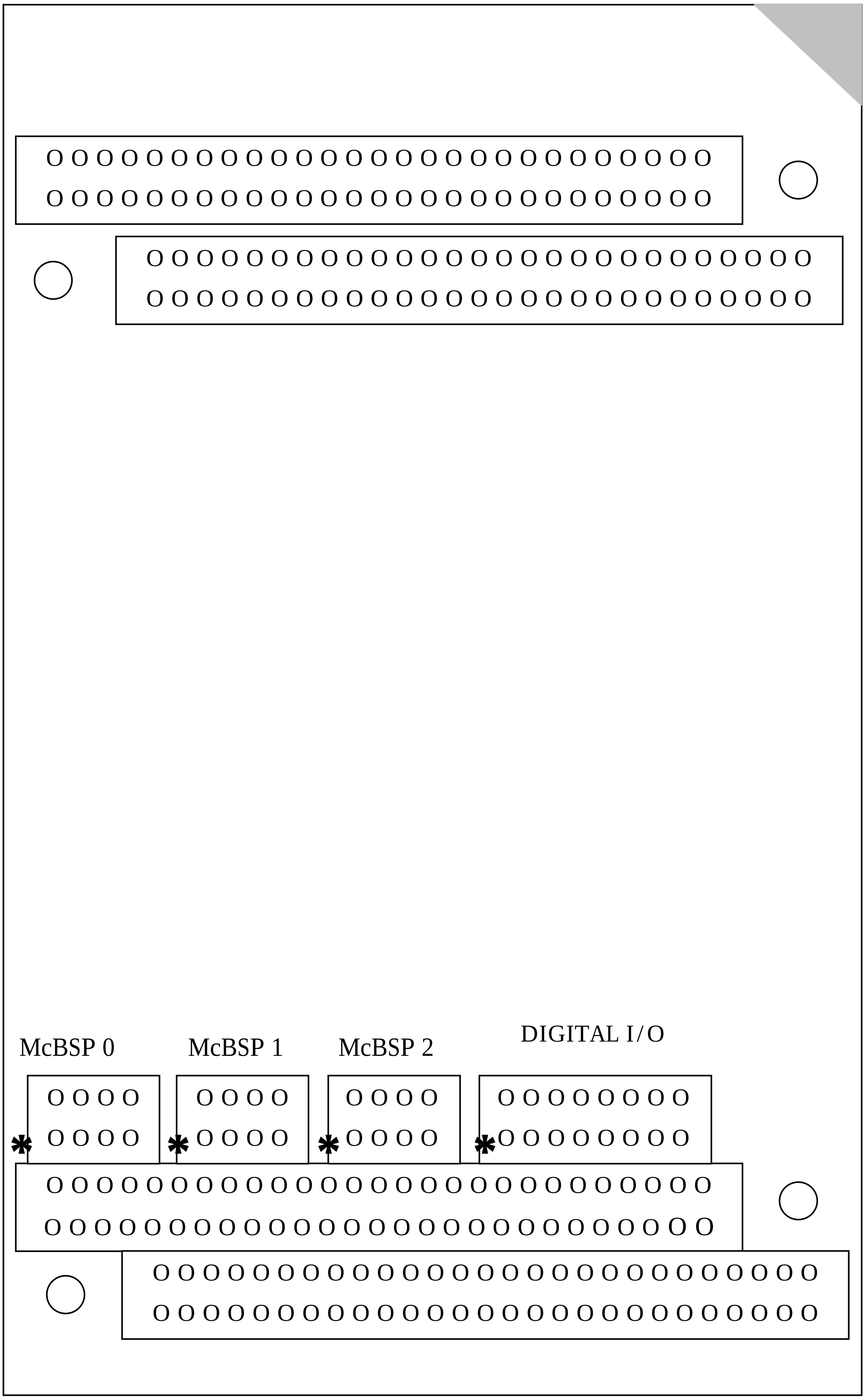
Positioning of C6000 processor module connectors

The connectors are aligned in pitch with the HERON connectors, and the centre of the lower pin of these connectors (as seen in the picture above) is exactly 2mm up from the centre of the topmost row of pins of the HERON connector.

The spacing between the connectors is exactly three pin pitches, i.e. the pitch would allow only two more pins to be fitted in the gap.

See the drawing on the next page.

All of the above connectors are optional, so might not be available on all HUNT ENGINEERING C6000 HERON modules. For example C6201/C6701 processors do not have McBSP2, so this connector will not be present.


McBSP 0
McBSP 1
McBSP 2
DIGITAL I/O