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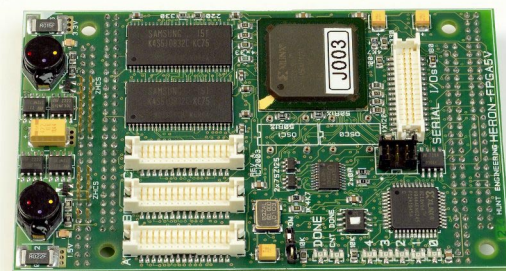
HERON-FPGA5 FPGA module with SDRAM and Digital I/O

- **Xilinx Virtex II FPGA with 1M gates.**
- **256Mbytes of SDRAM connected as 64Mx32 @133Mhz**
- **FPGA configuration downloaded using the HERON Serial Bus.**
- **Choice of clocking options**
- **45 user defined Digital I/Os**
- **2 channels of RS232/RS485**
- **Connects to all of the HERON FIFOs, UMI and module ID signals**
- **Flash PROM for storage of configuration data**

The HERON-FPGA5 provides a user programmable FPGA element for a HERON system combined with a bank of SDRAM capable of more than 500Mbytes/second. This can be used to process data flows or as a flexible digital I/O module.

Using the HERON serial bus allows the FPGA to be configured with a standard module configuration, or a custom one provided by the user, or HUNT ENGINEERING. After configuration the module can accept user messages over the HERON serial bus allowing registers etc to be programmed. If a more significant programming change is required a complete new FPGA configuration can be downloaded. The FLASH based configuration PROM can load the configuration data into the FPGA when it is used in an embedded system This PROM can be programmed using the standard JTAG cable available from Xilinx (such as Xilinx Parallel cable 3 or 4).

The Digital I/O has a number of voltage formats such as LVTTL or LVDS defined by the combination of a jumper setting and the configuration downloaded to the FPGA. In addition it is possible for the HERON-FPGA5 to be used as a choice of RS232, RS485 and Differential ECL serial interfaces.
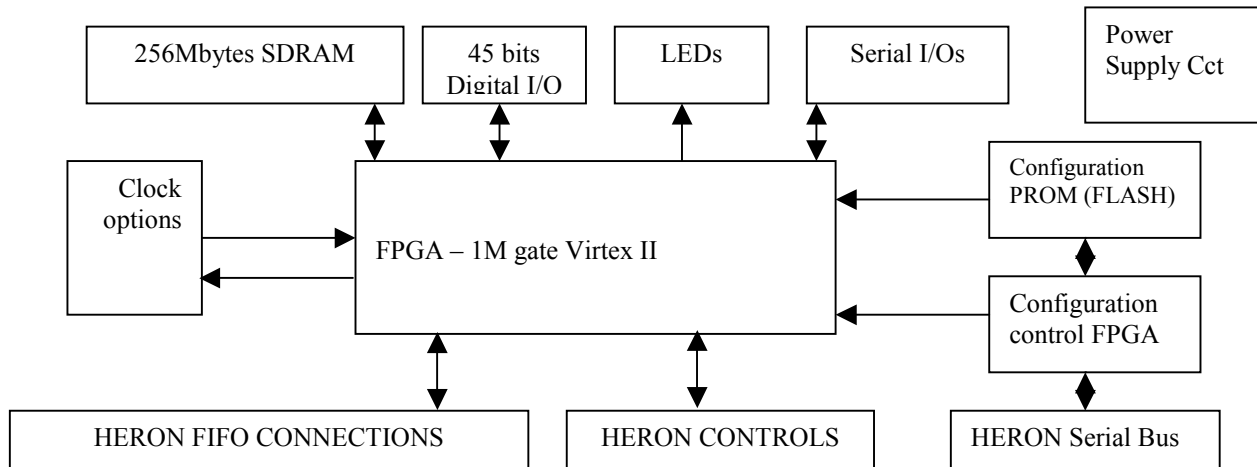
The HERON-FPGA5 can access HERON-FIFOs at a rate of 32 bits per FIFO clock in AND 32 bits per FIFO clock out concurrently. For example with a FIFO clock of 100Mhz this is 400Mbytes/sec in AND 400Mbytes/sec out

The module has a 100Mhz oscillator connected to the FPGA, which can be divided or multiplied using the Digital Clock Managers of the FPGA. Additionally there are sockets where the user can add further Oscillator modules for specialist frequencies or jitter/stability specifications. Of course the digital I/Os and UMIs can be used to provide external clock sources to the FPGA. The use of a Virtex II XC2V1000fg456-4 part allows clock rates of up to 365Mhz to be used internally in the FPGA, but the clock rate that can be used depends on the FPGA design you generate and must be determined using the FPGA development tools.

NOTE VIRTEX II I/Os are not 5v tolerant! Optional 100R series resistors can be fitted to make inputs 5V tolerant.

Block Diagram

| 256Mbytes SDRAM | 45 bits Digital I/O | LEDs | Serial I/Os | Power Supply Cct |

Clock options

FPGA – 1M gate Virtex II

Configuration PROM (FLASH)

Configuration control FPGA

| HERON FIFO CONNECTIONS | HERON CONTROLS | HERON Serial Bus |

Technical Specification

Processor:
Virtex II FPGA

Memory:
256Mbytes organised as 64M x 32 at 133Mhz

Host Bus:
HERON

Maximum Dimensions:
4.0 inches x 2.5inches x 6.5mm high.

Power requirements:
5V   dependent on FPGA configuration
 12V   Max: 0A
               Typ: 0A
-12V   Max:0A
               Typ:0A

FPGA Power Consumption/Dissipation
Max Bare FPGA package dissipation: 2.4W

From 5V supply :
FPGA PSU power can source 14.29W
Rest of logic uses 0.6W

Clocking Speed:
Max 365Mhz

I/O bandwidth:
e.g. HEPC9 400Mb/s in + 400Mb/s out

Software

Xilinx ISE series tools are required to make a new FPGA configuration.
HUNT ENGINEERING provides software to download the FPGA configuration file onto the hardware, plus configuration examples.
HUNT ENGINEERING may offer to provide your configuration file for you, but this may be chargeable.

Applications
These fast FPGAs can be used for DSP processing tasks at very high clock rates.
Alternatively the HERON-FPGA5 can be used to provide custom digital I/O perhaps combined with signal generation, storage and pre-processing.

Related Products
HEPC9 – PCI Heron Module carrier
HERON1-DSP module
HERON4 – DSP module
HEGD series I/O modules

Ordering Information

HERON-FPGA5V
    1M gates Virtex II version

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