

HUNT ENGINEERING

Chestnut Court, Burton Row, Brent Knoll, Somerset, TA9 4BP, UK Tel: (+44) (0)1278 760188, Fax: (+44) (0)1278 760199,

Email: sales@hunteng.co.uk URL: http://www.hunteng.co.uk http://www.hunt-dsp.com





'one of the many tools we have to help us build your system solution'



HERON-FPGA4V FPGA module with Digital I/O

- Xilinx Virtex II FPGA with 3M 6M or 8M gates
- FPGA configuration downloaded using the HERON Serial Bus or from on board FLASH PROM.
- Choice of clocking options
- 90 user defined Digital I/Os
- Several serial I/O options possible -- configured by the FPGA.
- Connects to all of the HERON FIFOs, UMI and module ID signals

The HERON-FPGA4 provides a user programmable FPGA element for a HERON system. This can be used to process data flows or as a flexible digital I/O module.

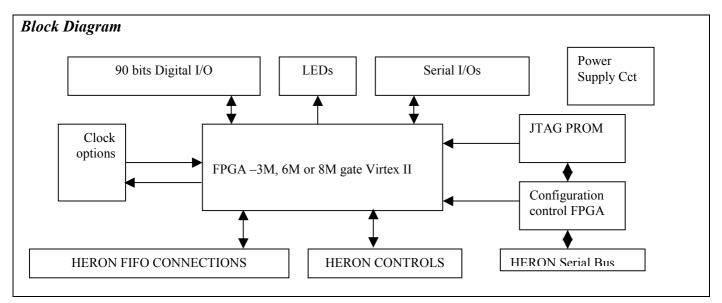
Using the HERON serial bus allows the FPGA to be configured with a standard module configuration, or a custom one provided by the user, or HUNT ENGINEERING. After configuration the module can accept user messages over the HERON serial bus allowing registers etc to be programmed. If a more significant programming change is required a complete new FPGA configuration can be downloaded. The FLASH based configuration PROM can load the configuration data into the FPGA when it is used in an embedded system This PROM can be programmed using the standard JTAG cable available from Xilinx (such as Xilinx Parallel cable 4 or USB-JTAG cable).

The Digital I/O has a number of voltage formats such as LVTTL or LVCMOS defined by the combination of a jumper setting and the configuration downloaded to the FPGA. In addition it is possible for the HERON-FPGA4 to be used as a choice of RS232, RS485 and Differential ECL serial interfaces.

The HERON-FPGA4 can access HERON-FIFOs at a rate of 32 bits per FIFO clock in AND 32 bits per FIFO clock out concurrently. For example with a FIFO clock of 100Mhz this is 400Mbytes/sec in AND 400Mbytes/sec out.

The use of a Virtex II XC2V*000-*ff1152 part allows clock rates of up to 365Mhz, and also provides hard coded multipliers and extended I/O formats such as Low Voltage Differential Signalling (LVDS)

NOTE VIRTEX II I/Os are not 5v tolerant! Optional 100R series resistors can be fitted to make inputs 5V tolerant.



Technical Specification	Software	Ordering Information
Processor:		0
Virtex II FPGA	Xilinx Foundation series tools are	HERON-FPGA4V3000-5 = $3M$ gates,
	required to make a new FPGA	speed grade 5
Memory:	configuration.	HERON-FPGA4V6000-4 = $6M$ gates,
None external to FPGA	HUNT ENGINEERING provides	speed grade 4
	software to download the FPGA	HERON-FPGA4V6000-5 = $6M$ gates,
Host Bus:	configuration file onto the hardware,	speed grade 5
HERON	plus configuration examples. HUNT ENGINEERING may offer to	HERON-FPGA4V8000-5 = 8M gates, speed grade 5
Maximum Dimensions:	provide your configuration file for you,	speed grade 3
4.0 inches x 2.5inches x 6.5mm high.	but this may be chargeable.	
1.0 menes x 2.5 menes x 0.5 mm mgm.	out this may be chargeable.	
Power requirements:	Applications	
5V dependent on FPGA configuration	These fast FPGAs can be used for DSP	
12V Max: 0A	processing tasks at very high clock	
Typ: 0A	rates.	
-12V Max:0A	Alternatively the HERON-FPGA4 can	
Typ:0A	be used to provide custom digital I/O	
	perhaps combined with signal generation of pre-processing.	
FPGA Power Consumption/Dissipation Max Bare FPGA package dissipation: 4.5W	generation of pre-processing.	
Wax Bare 11 GA package dissipation. 4.5 w	Related Products	
From 5V supply: up to 17.8 with heatsink	HEPC9 – PCI Heron Module carrier	
and fan options	HERON4 – DSP module	
FPGA PSU power can source 18.39W	HEGD series I/O modules	
Rest of logic uses 0.8W		
Clocking Speed:		
Max HERON-FPGA4 365Mhz		
I/O bandwidth:		
e.g. HEPC9 400Mb/s in + 400Mb/s out		

HUNT ENGINEERING acknowledges all Trademarks used in this document. This document does not form part of a contract, HUNT ENGINEERING reserves the right to change product specifications without notice and to refuse to supply any item detailed on this data sheet E&OE.

Distributor details: